

Compal Confidential

Hasswell M/B Schematics Document

Intel ULV Processor with LPDDR3/DDRIIIL

Date : 2013/06/26

Version 1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Cover Page
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Compal Confidential
Model Name : Haswell

File Name :
LA-9314PR10(NonCS)

(nonCS)

WLAN(MiniPCIe slot) P23

Port 3

Port 3 (Reserved) USB2.0
480Mb/s

(NonCS:USB)

Touch screen
P20

Port 5 USB2.0
480Mb/s

(NonCS)

Int.KBD

Touch Pad

FAN

Lid switch

Accelerometer
HP3DC2 P46

PS2

ENE KB9012
P42

SMBUS
100KHz

SPI ROM
8M P7

Haswell
Ultra Light & Thin
1168P BGA
(USW ULT)

VRAM
P37~P40

Nvidia
N14-GV2
17W
P32~P36

PCI-Ex4
Lane 7-Lane10
PCIe 2.0:5Gb/s
PCIe 3.0:8Gb/s

LVDS panel
P20

RTD2136S
P18

eDPx2
2.7Gb/s

HDMI Conn
DDPB port P19

HDMI
222.75MHz

PCI-E Card reader
RTS5237 P25

Lane 4 PCI-E

PCIe 1.0:2.5Gb/s
PCIe 2.0:5Gb/s

10/100/1G LAN
RTL8161G P24

Lane 5

PCIe 1.0:2.5Gb/s
PCIe 2.0:5Gb/s

Lane 11 PCIe 1.0:2.5Gb/s
PCI-E

SPI
50MHz

SPI ROM
8M P7

Dual Channel

DDR3-SO-DIMM X 2
P15,16 (nonCS)

DDR3L 1333MHz 1.35V

SATA 3.0 Port 2

2.5" SATA HDD P22

GEN1 1.5Gb/s
GEN2 3Gb/s
GEN3 6Gb/s

Port 3

SSD(MiniPCIe slot) P22

USB3.0
5Gb/s

USB2.0 Port 0

480Mb/s

Port 1

USB2.0 port P26

Port 2

USB2.0 port P26

Port 1

USB2.0 port P26

Port 2

USB2.0 port P26

Port 4

USB charger P27

USB2.0 port

Port 6

Camera P20

WWAN(NGFF_B) P21

SIM conn

HDA 24MHz

HDA Audio codec
92HD91 P28

Audio Sub P29

Sub conn

SMBUS 1MHz

HP Amp P30

HP&MIC jack

(nonCS)

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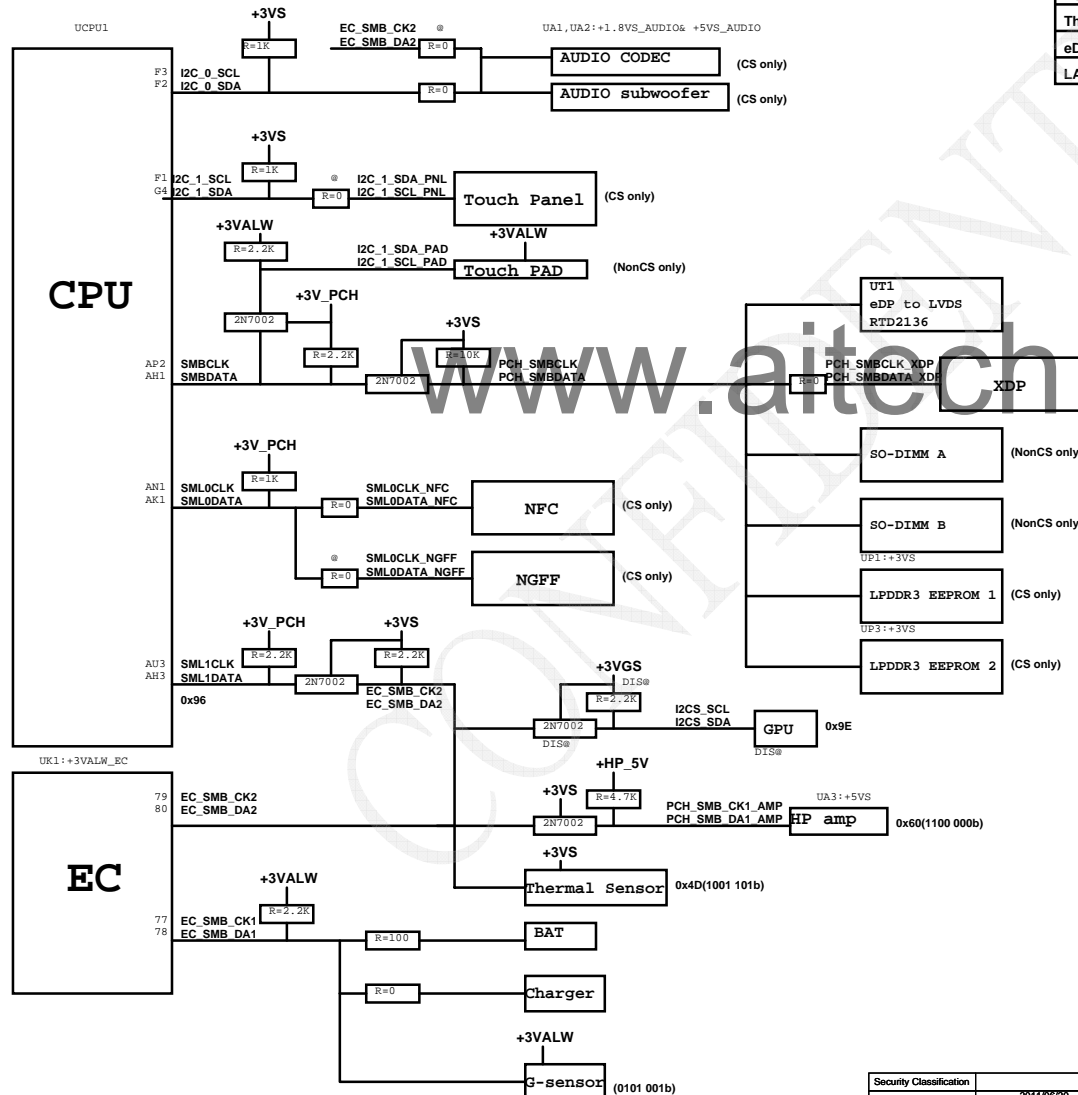
Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
B+	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VALW_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.05V	SUSP#	
+1.8V	SYSON	PM_SLP_S5# / PM_SLP_S4#
+1.2V_1.35V	SYSON	PM_SLP_S5# / PM_SLP_S4#
+5VS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.8VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+1.05VS_MODPHY	X	MPHY_PWREN
+0.6V_0.675VS	X	SM_PG_CTRL
+VCC_CORE	X	VR12.5_VR_ON

@ is NO SMT part (empty)
short@ : short pad , don't pop.
@EMI@, @ESD@, @RF@ : Reserve , don't pop.

RF@ : RF team request, must add.
EMI@ : EMI team request, must add.
ESD@ : ESD team request, must add.
LVDS@ : Support LVDS panel.
eDP@ : Support eDP panel.
DIS@ : GPU BOM config.
WWAN@ : For WWAN function.
VGU00@, VGU11@ : Board ID config.

<Power gating GPIO, wake ,INT and RST>

Device	Power gating GPIO	Enable (ON) CPU IC HW part	RST/IRQ	Wake/INT
NGFF SSD	X(Not support)			
NGFF WWAN	X(Not support)			
NGFF WLAN/BT				
WLAN (MiniPCIe) *	GPIO83	H H Load switch	GPIO34 *	GPIO54 *
USB3.0 CONN	GPIO13	L L USB switch		
USB3.0 CONN(Charger)	GPIO43	H H USB charger		
Card reader (PCI-E)	GPIO60	H H Load switch	GPIO93	GPIO94
USB2.0 Camera	GPIO25	H H Load switch		
Touch Panel	GPIO89	H H Load switch	GPIO52	GPIO50
Touch Pad -NonCS				
Touch Pad -CS *	GPIO88	L L PMOS		GPIO55 *
WWAN	GPIO84	H H Load switch		
SATA HDD/SSD	GPIO90	H H Load switch	GPIO38 X(Not support)	
mSATA	GPIO86	H H Load switch	DEVSLP2#/GPIO39	
Audio DSP + codec	GPIO76	H H Load switch	X(Not support)	
Thermal (EC)	X(Not support)			
eDP*	V	Load switch		
LAN (PCI-E)	GPIO12	H L Load switch	GPIO91	GPIO92

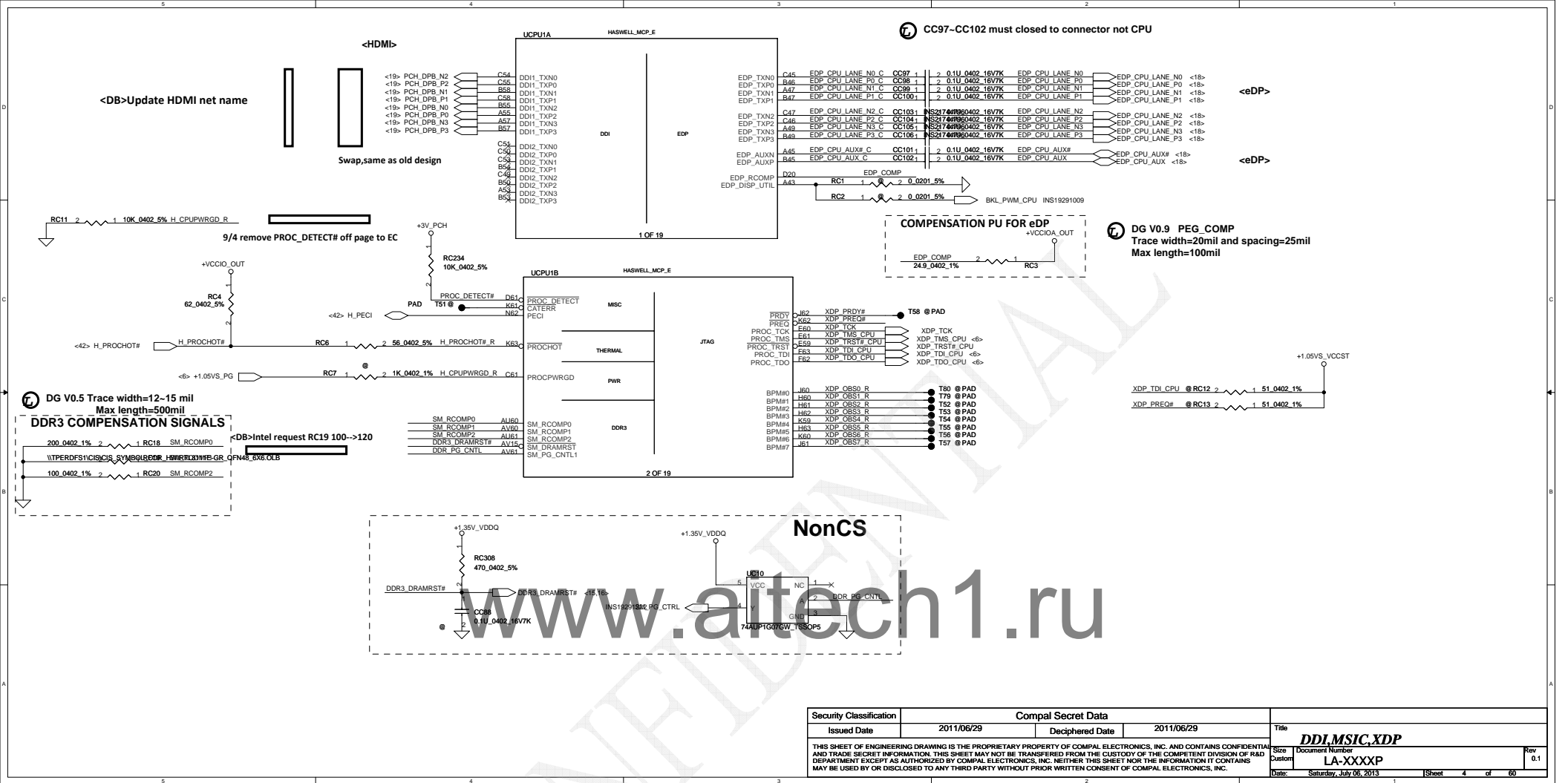


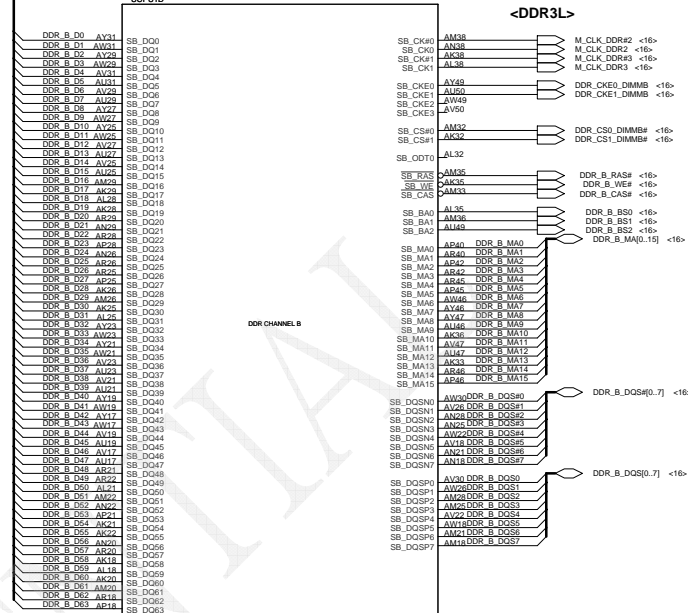
<USB2.0 port>

USB2.0 port	DESTINATION CS	NonCS
0	USB 2.0(left side)	USB 2.0(left side)
1	USB 2.0(left side)	USB 2.0(left side)
2	USB 2.0(right side)	USB 2.0(right side)
3	WLAN (NGFF)	WLAN (MiniPCIe)
4	Camera	Camera
5	No contact	Touch screen
6	WWAN	WWAN
7	Finger printer	Finger printer

<PCI-E, SATA, USB3.0>

Lane#	PCI-E	SATA	USB3.0	DESTINATION CS	NonCS
1			1	USB3.0	USB3.0
2			2	USB3.0	USB3.0
3	1		3	X(Not support)	X(Not support)
4	2		4	Card reader(PCI-E)	Card reader(PCI-E)
5	3			10/100/1000 LAN	10/100/1000 LAN
6	4				
7					GPU(DiS only)
8					GPU(DiS only)
9					GPU(DiS only)
10					GPU(DiS only)
11	L3	3		WLAN (NGFF)	WLAN (MiniPCIe)
12	L2	2		X(Not used)	X(Not used)
13	L1	1		SSD(mSATA)	SSD(mSATA)
14	L0	0		2.5"HDD	2.5"HDD



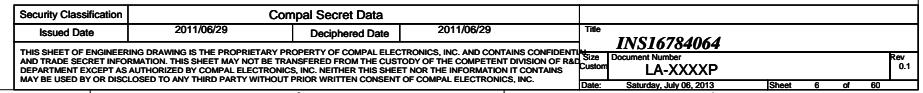


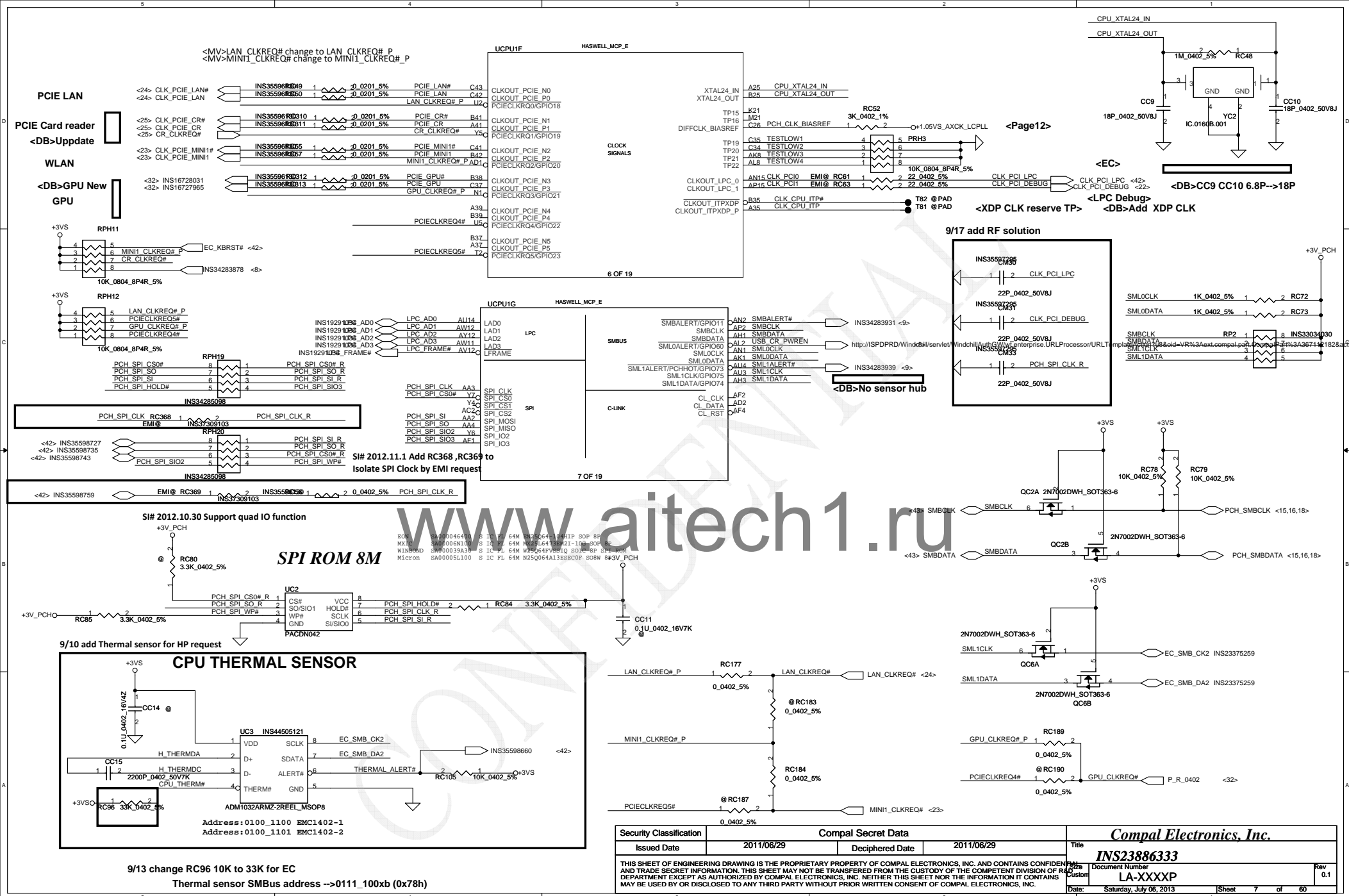
4 OF 19

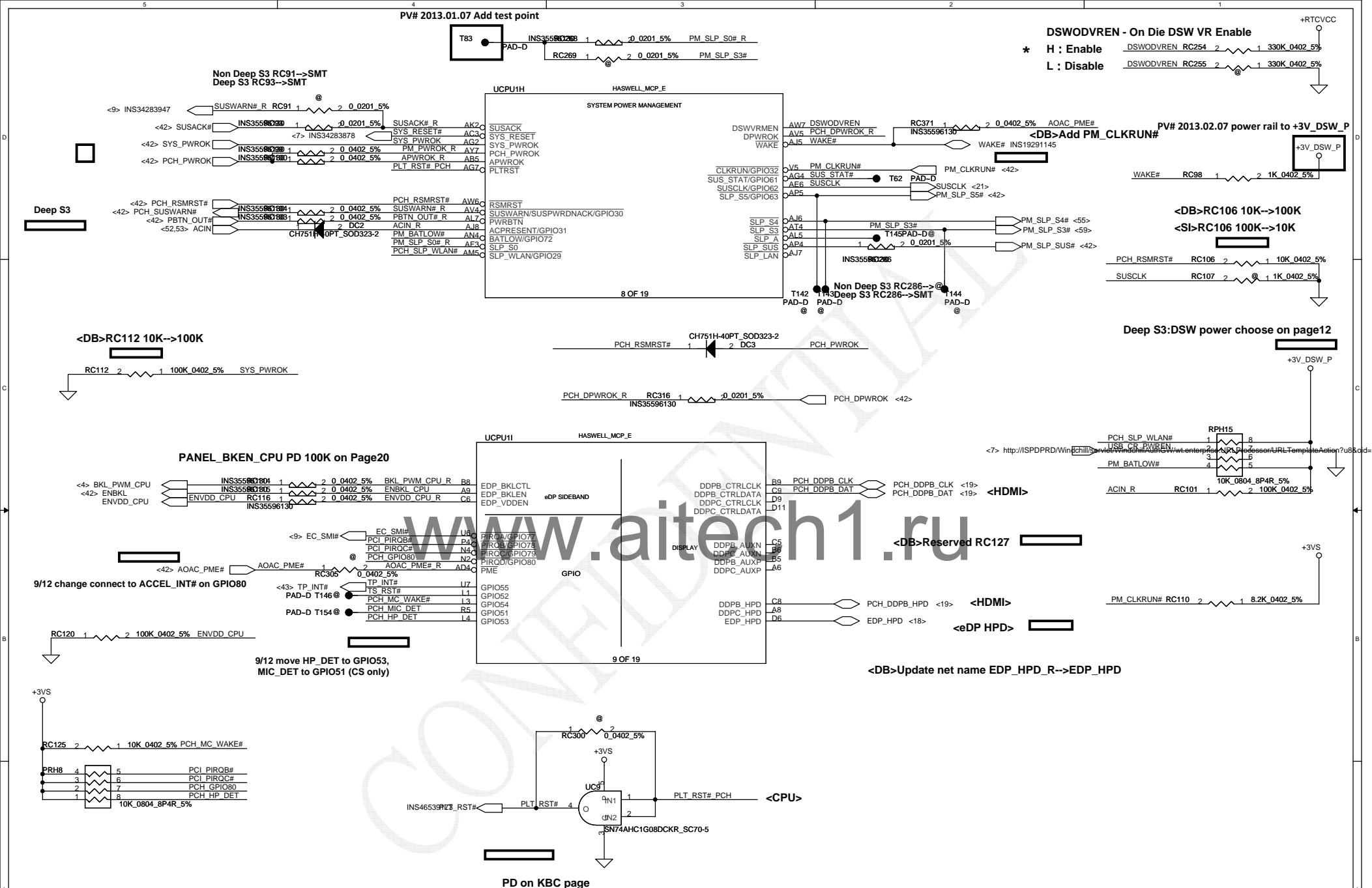
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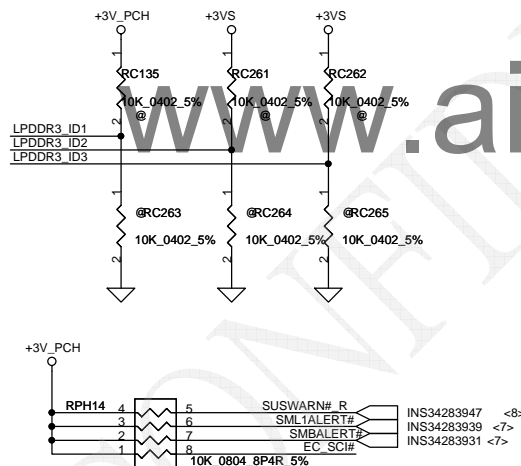
Compal Electronics, Inc.







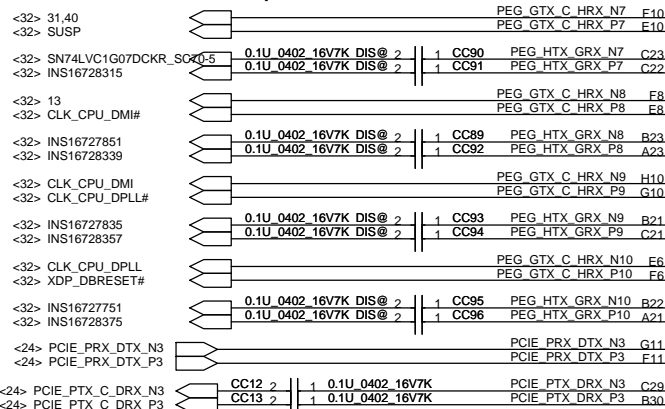
Security Classification	Compal Secret Data			<div> <div>Title</div> <div> PM,GPIO,DDI </div> </div> <div> <div>Size</div> <div>Document Number</div> <div> LA-XXXXP </div> </div> <div> <div>Date</div> <div>Saturday, July 06, 2013</div> <div> <div>Sheet</div> <div>8</div> <div>of</div> <div>60</div> </div> </div> <div> <div>Rev</div> <div>0.1</div> </div>		
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GPI027	RC277	1	2	10K 0402 5% EC PME#
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Security Classification	Compal Secret Data					
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	GPIO,UART,I2C	
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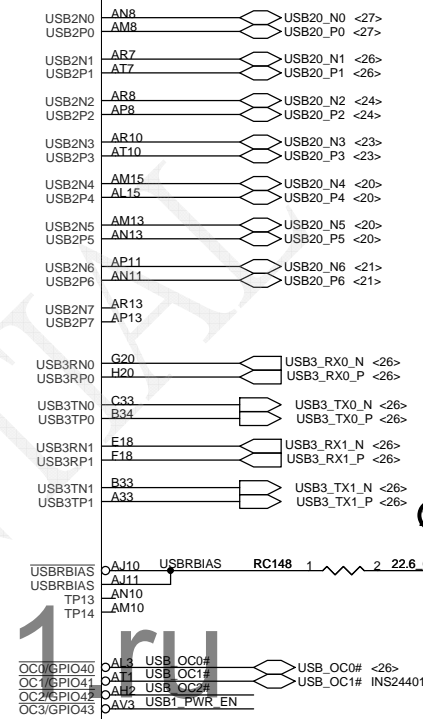
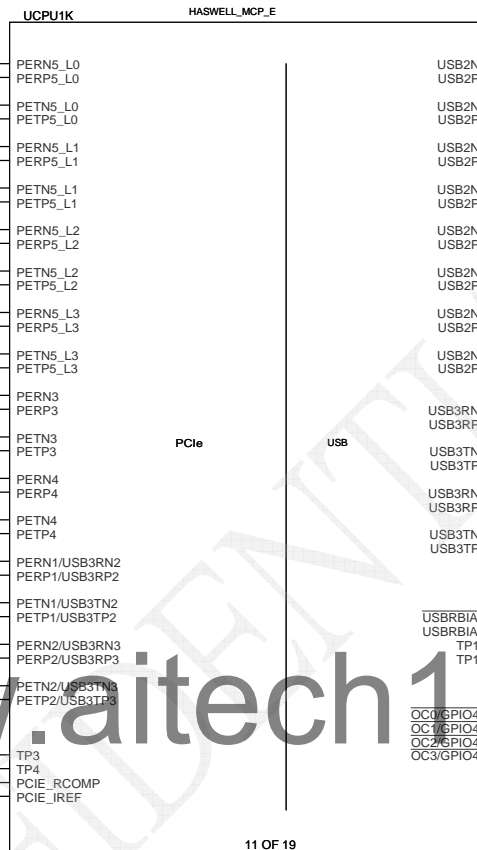
Check with intel PEG which port



<DB>Del from JIO1.

<Page12>

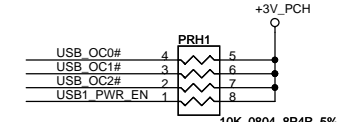
DG V0.9 PCIE_RCOMP
Width=12mil,spacing=12mil
Max length=500mil



USB2.0/USB3.0
USB2.0/USB3.0
USB2.0 <DB>IO board
WLAN/BT (NGFF)
Camera
Touch screen <DB>NonCS only
WWAN <DB>Add WWAN

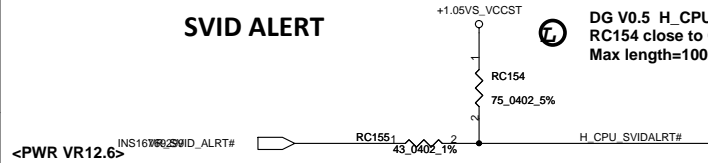
USB2.0/USB3.0
USB2.0/USB3.0
DG V0.9 USBRBIAS
Trace width=50ohm and spacing=15mil
Max length=500mil

<DB>Remove RC149 and RC150 @ part

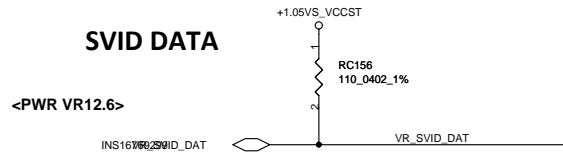


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SVID ALERT

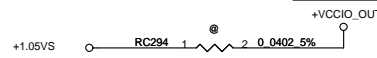


SVID DATA

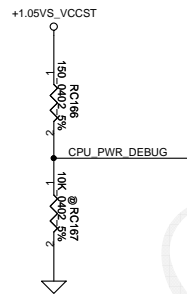


+VCCIO_OUT power rail choose

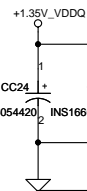
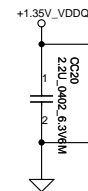
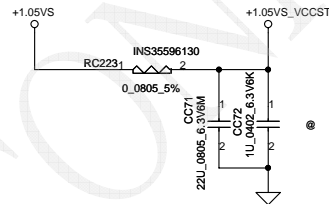
<CPU>



DG V0.5 VIDSOUT
RC156 close to CPU<500mil
Max length=1000~2000mil

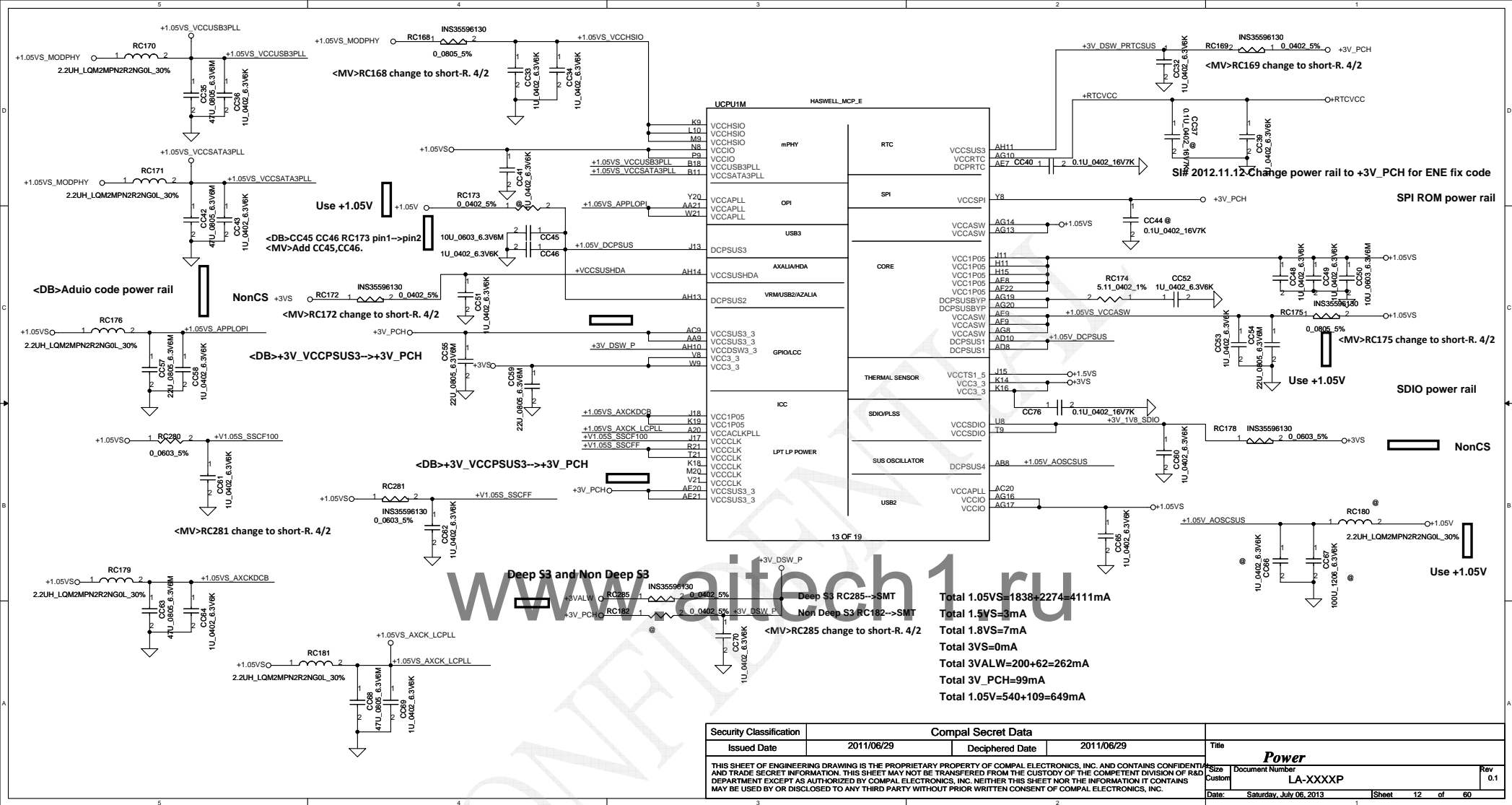


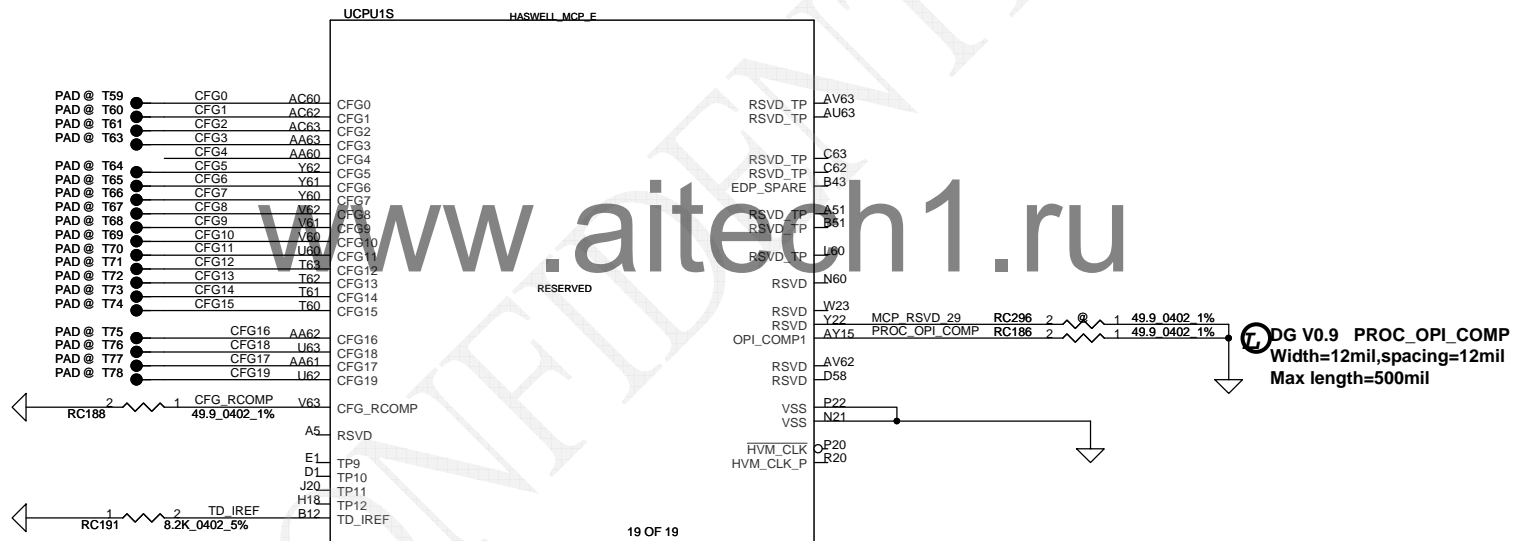
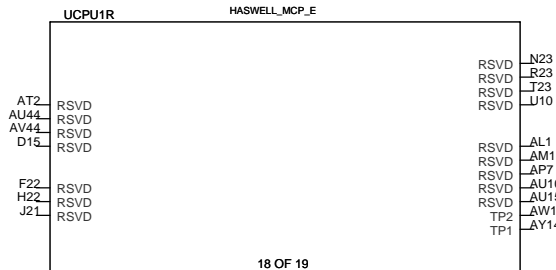
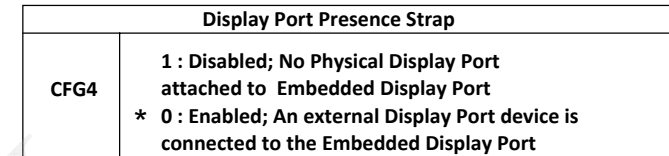
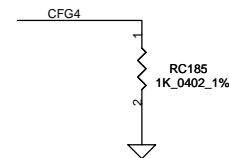
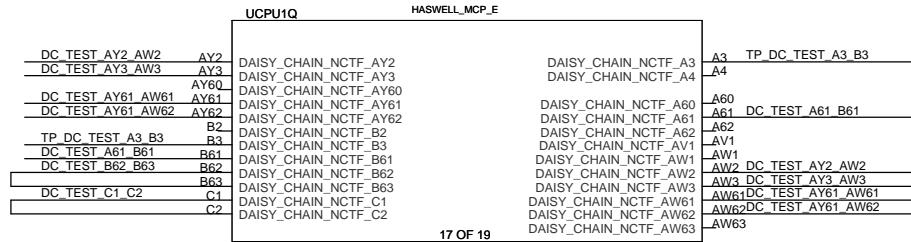
<MV>RC223 change to short-R. 4/2



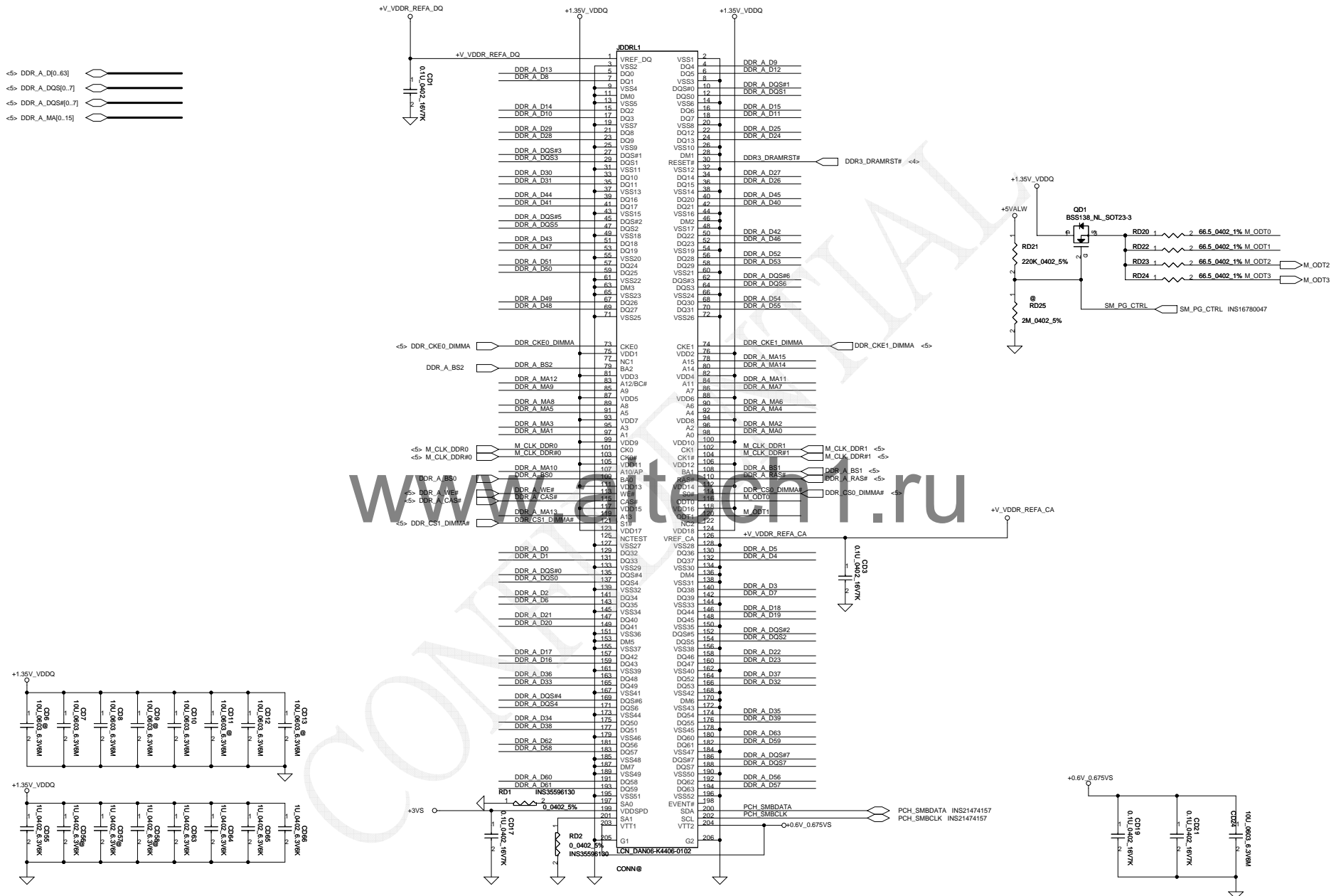
<DB>intel define 470u, ESR12mohm

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				LA-XXXXP
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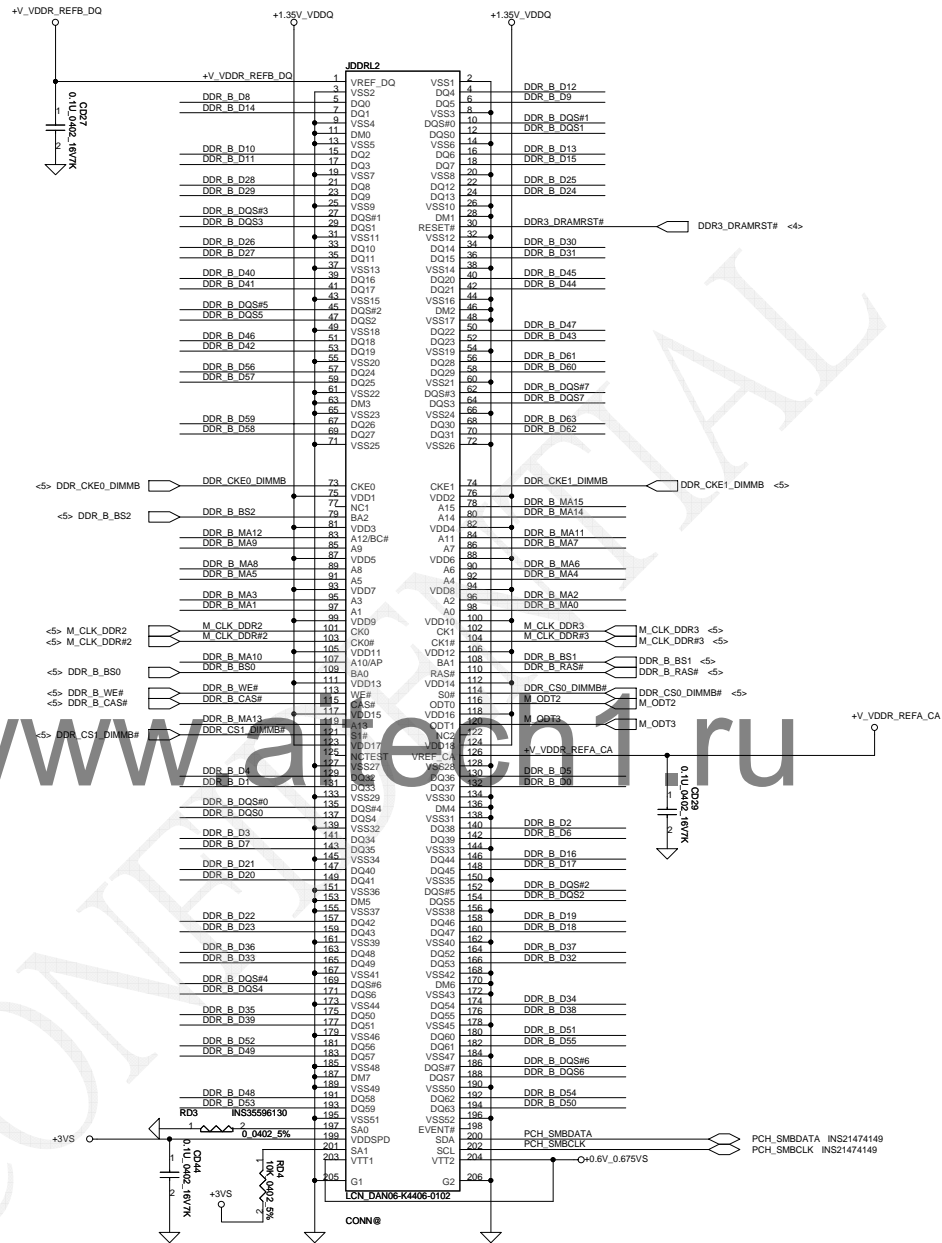


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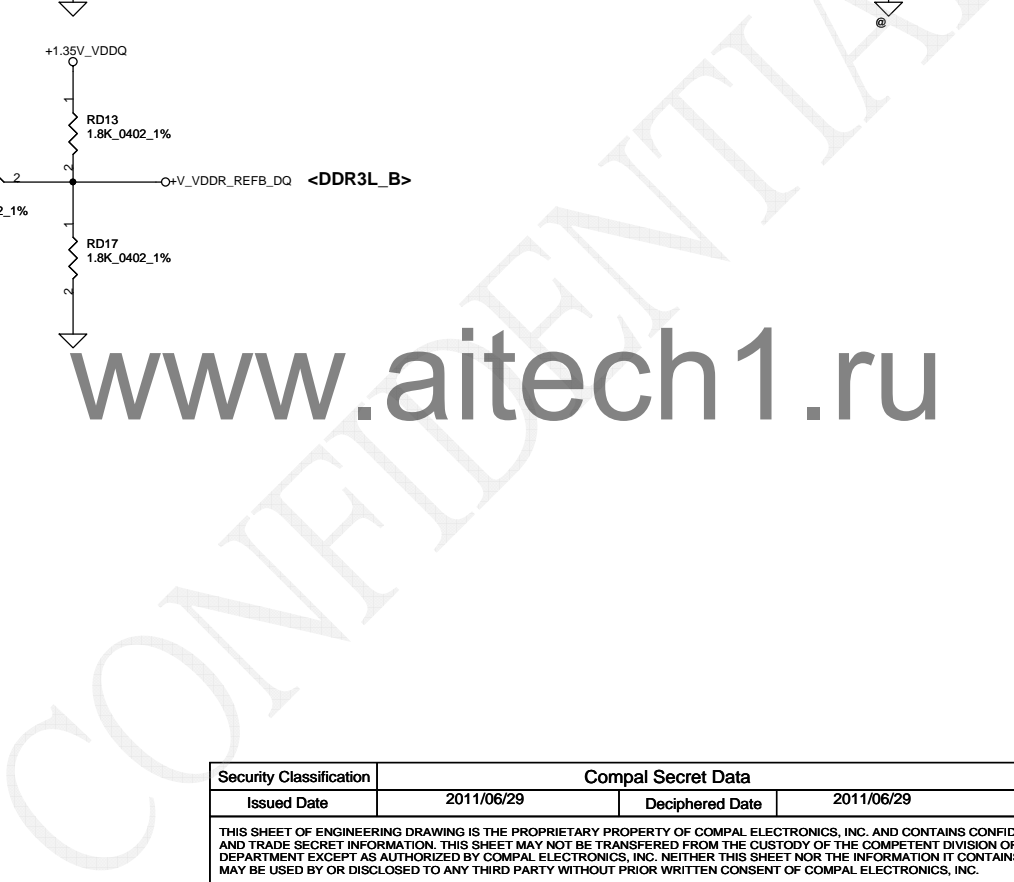


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		LA-XXXXP		0.1	
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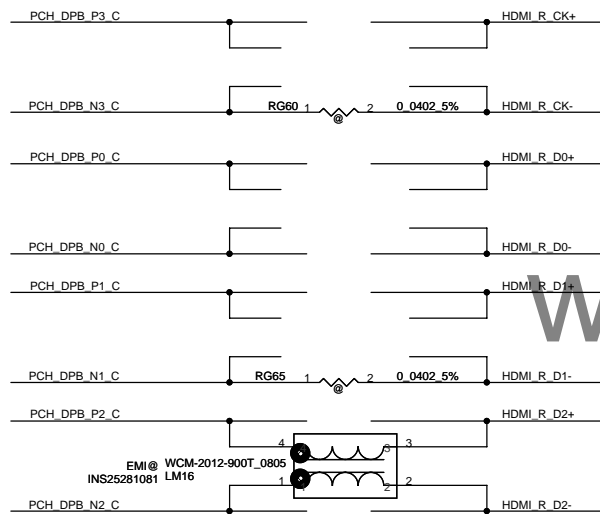
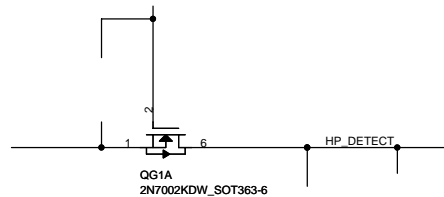
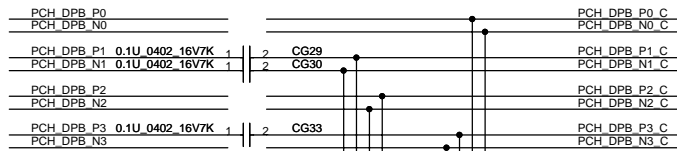
<5> DDR_B_D[0..63]
 <5> DDR_B_DQS[0..7]
 <5> DDR_B_DQS#0..7
 <5> DDR_B_MA[0..15]



+1.35V_VDDQ
RD13
1.8K_0402_1%
2
O+V_VDDR_REFB_DQ <DDR3L_B>
RD17
1.8K_0402_1%

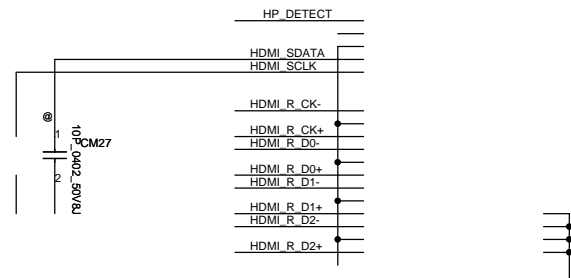
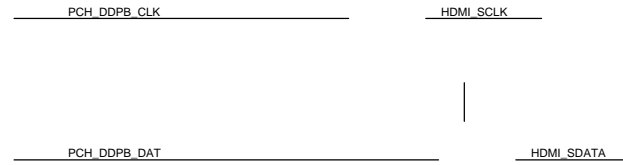


+1.35V_VDDQ
RD13
1.8K_0402_1%
2
O+V_VDDR_REFB_DQ <DDR3L_B>
RD17
1.8K_0402_1%

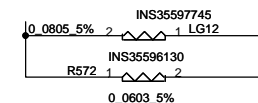
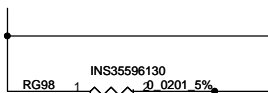


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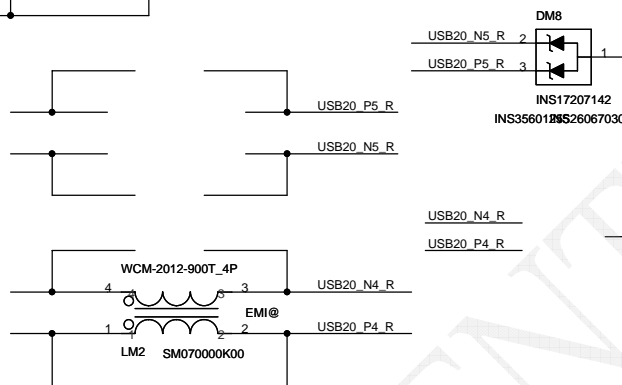
HDMI SDATA
HDMI SCLK
PCH DDPB CLK
PCH DDPB DAT



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D_MIC_CLK
D_MIC_DATA



LVDS A TXOUT0-
LVDS A TXOUT0+
LVDS A TXOUT1-
LVDS A TXOUT1+
LVDS A TXOUT2-
LVDS A TXOUT2+
LVDS A TXCLK+
LVDS A TXCLK-

LVDS B TXOUT0-
LVDS B TXOUT0+
LVDS B TXOUT1-
LVDS B TXOUT1+
LVDS B TXOUT2-
LVDS B TXOUT2+
LVDS B TXCLK+
LVDS B TXCLK-

LVDS PWM
LVDS BKL TEN

USB20 N5 R
USB20 P5 R

USB20 N4 R
USB20 P4 R

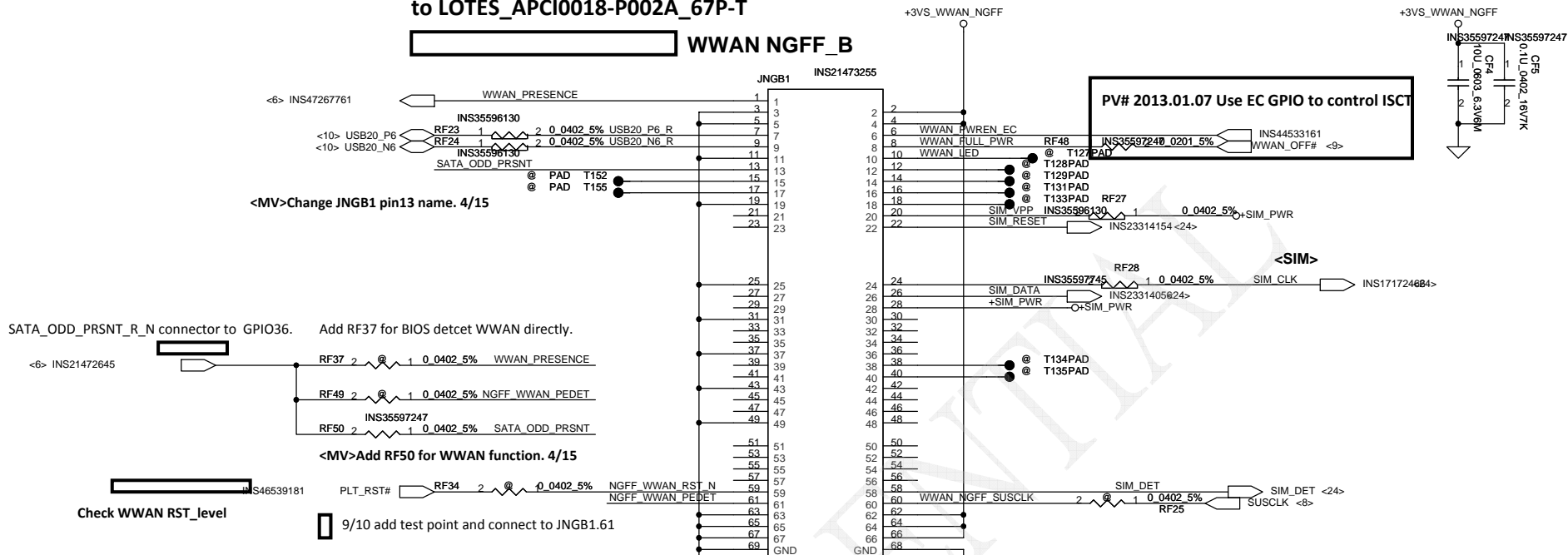
D MIC CLK
D MIC DATA

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Issued Date	2011/03/10	Deciphered Date	2009/06/22	Title	SEN70069
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				Date: Saturday, July 06, 2013	Rev 0.1
				Sheet 20 of 60	

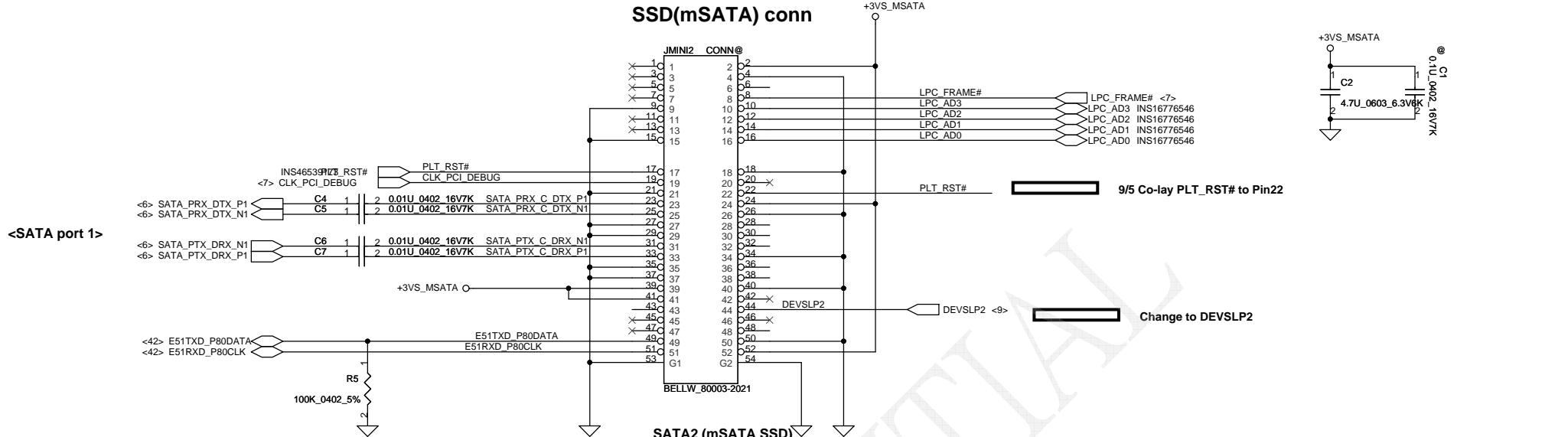
8/27 Change connector footprint to LOTES_APCI0018-P002A_67P-T

WWAN NGFF_B

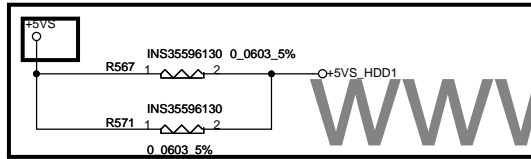


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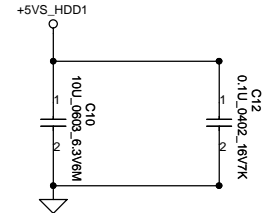
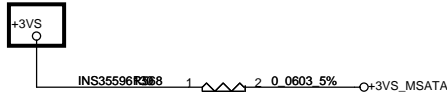
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Issued Date	2011/06/30	Deciphered Date	2013/06/30	Title	WWAN NGFF
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				Date: Saturday, July 06, 2013	Sheet 21 of 60



9/5 change Q23 +5VALW/+3VALW to +5VS/+3VS

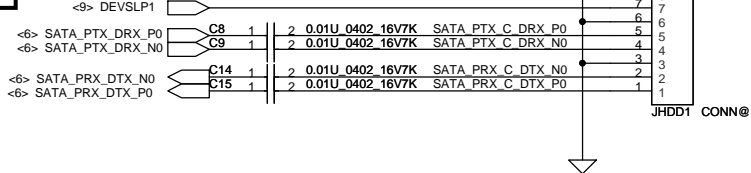


PV# 2013.01.24 Add R572 to support HDD heavy loading current .



SATA 1 (2.5" HDD and SSD)

<SATA port 0>



<DB>Change to 10 Pin **2.5" HDD Conn.**

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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	S CER CAP 10U 10V Z Y5V 0805
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				Date	Saturday, July 06, 2013
				Sheet	22 of 60
				Rev	0.1

INS35596130_0201_5%
LAN_CLKREQ# 2 1 LAN_CLKREQ# R

INS35596130
RL11 1 0.0201_5%
LANWAKEB LAN_WAKE#

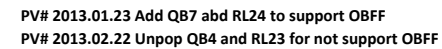
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USB20_N2
USB20_P2
SIM_CLK
SIM_DATA
SIM_DET
SIM_RESET

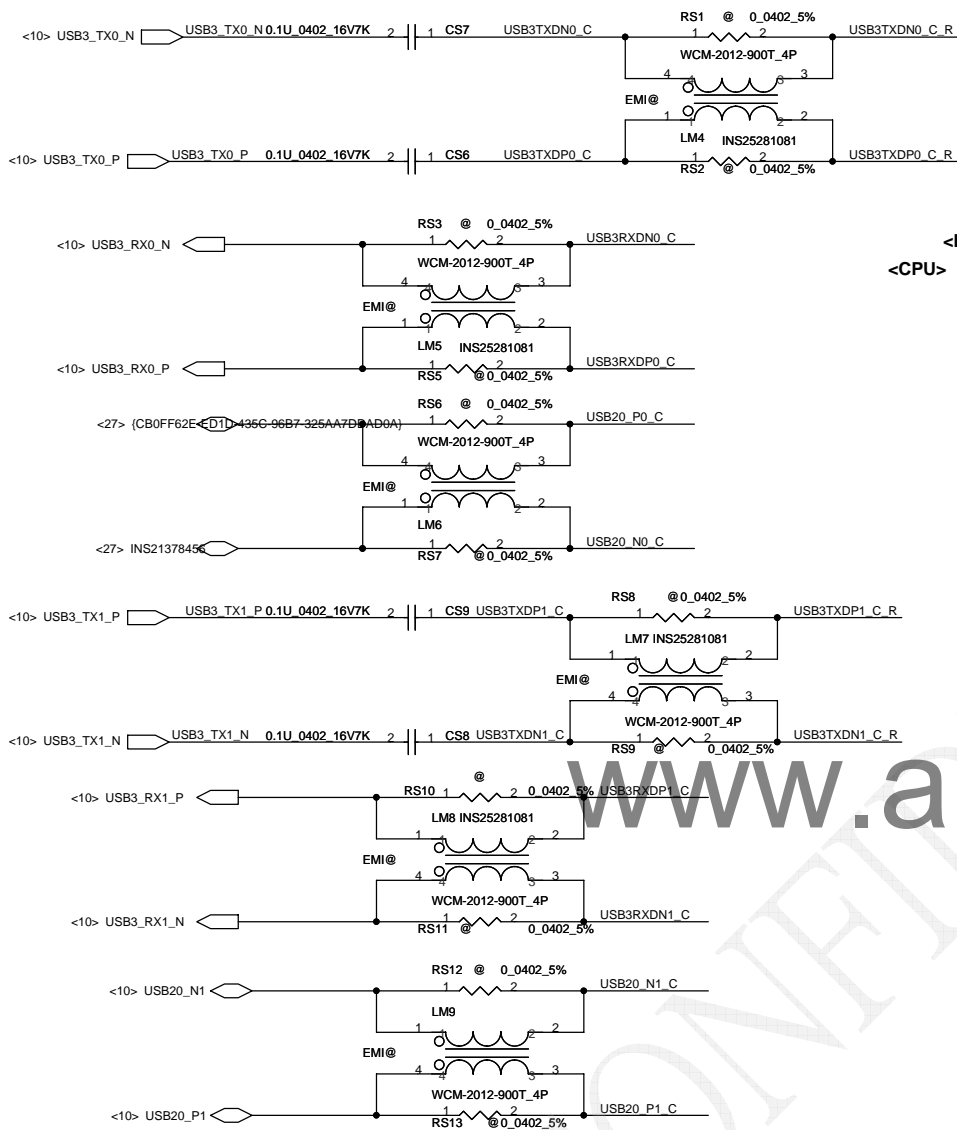
WAKE# LAN_WAKE#
QBS
2N7002H_SOT23-3

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Issued Date	2011/06/29	Deciphered Date	2011/0/03	Title	LAN 8111G
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				Date	Saturday, July 06, 2013
				Sheet	24 of 60
				Rev	0.1

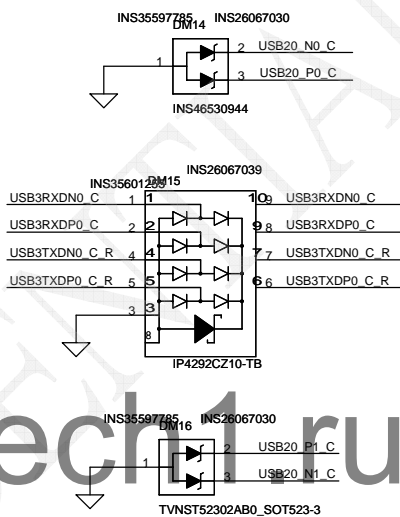
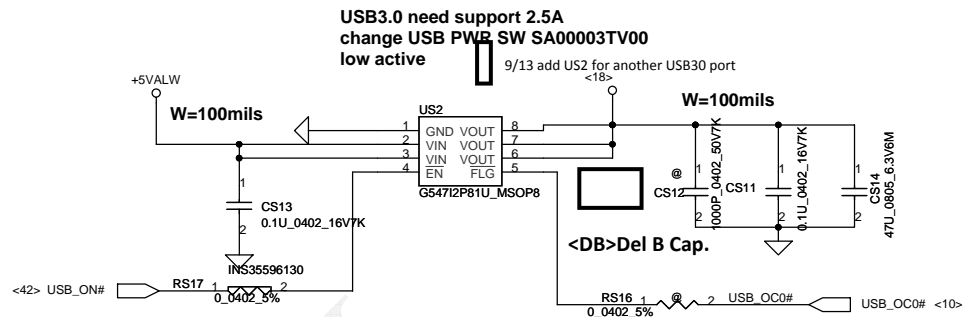
9/4 Modify JP10 connector pin defined



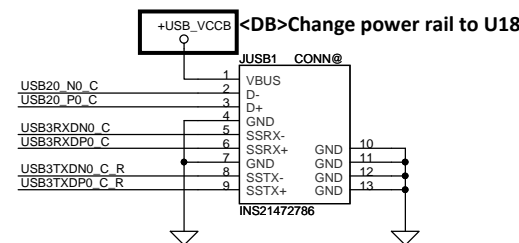
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	C8050Y106Z010T
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				Docu- ment Number	0.1
				LA-XXXXP	
Date: Saturday, July 06, 2013				Sheet	25 of 60



<EC>
<CPU>

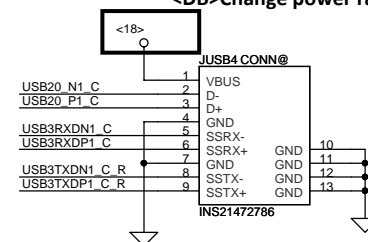


<DB>Update footprint to DC233008M10.
USB2.0/USB3.0 port 1



USB2.0/USB3.0 port 2

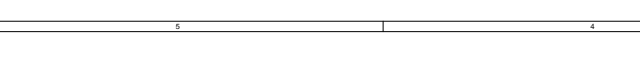
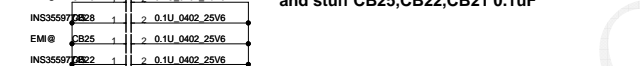
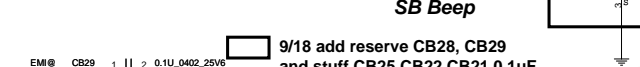
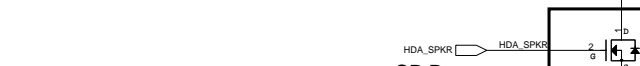
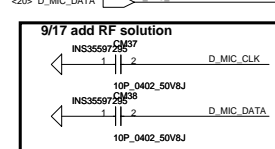
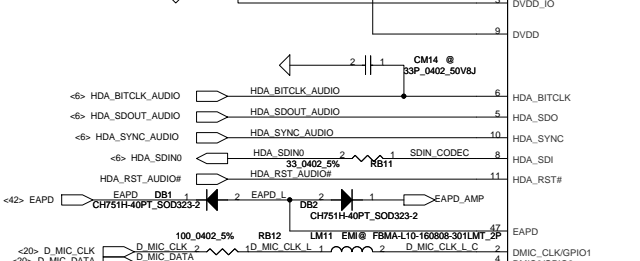
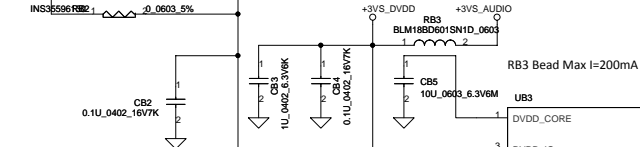
<DB>Change power rail to U18.



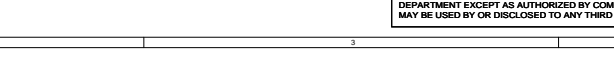
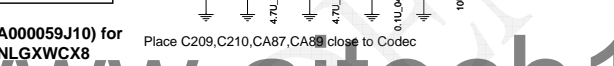
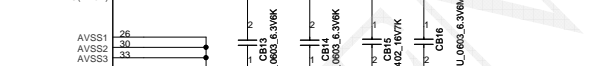
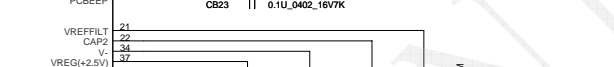
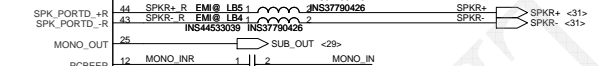
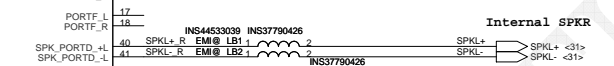
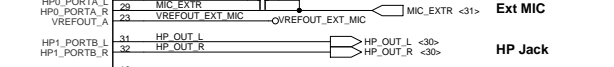
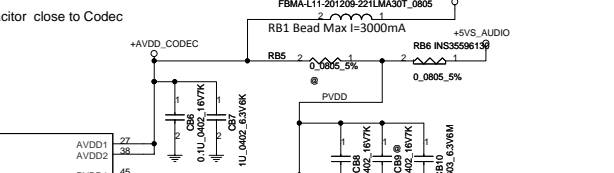
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				Date: Saturday, July 06, 2013	Sheet 26 of 60

DVDD_IO should match
with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)

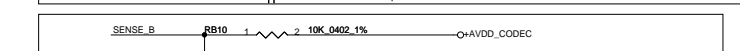
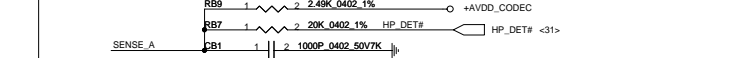
Place AVDD, PVDD, and DVDD capacitor close to Codec



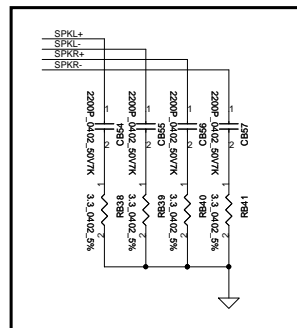
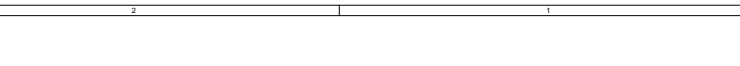
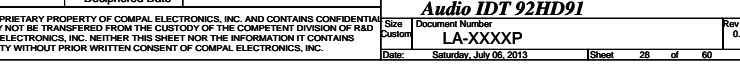
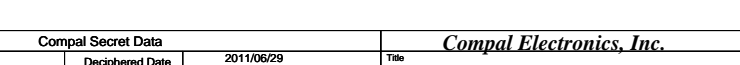
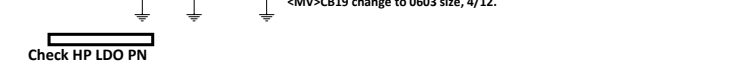
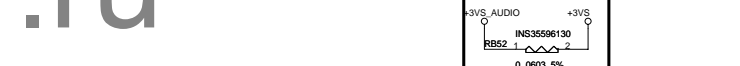
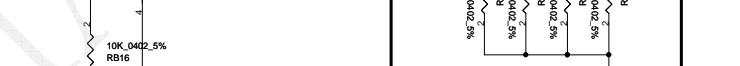
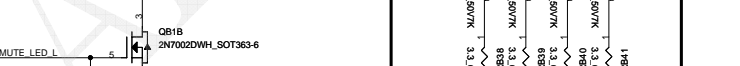
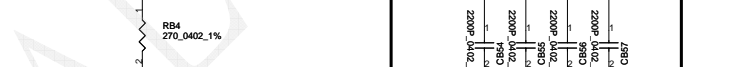
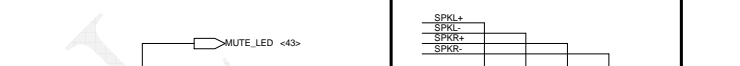
Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals



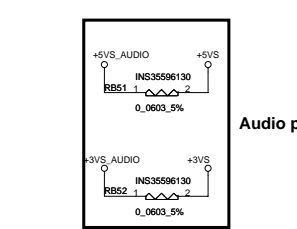
PLACE CLOSE TO U1 PIN 13



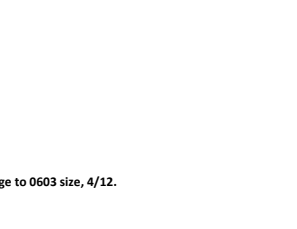
PLACE CLOSE TO U1 PIN 14



Place need close UB3



Audio power



Audio power

Ext MIC

HP Jack

Internal SPKR

Internal SPKR

Internal SPKR

Internal SPKR

Internal SPKR

Internal SPKR

Internal SPKR

Internal SPKR

Internal SPKR

Internal SPKR

Internal SPKR

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Internal SPKR

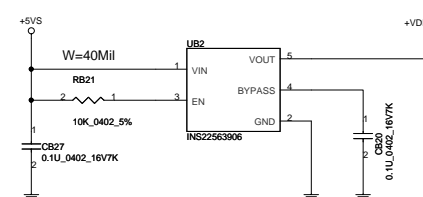
Internal SPKR

Internal SPKR

Internal SPKR

SB Bleep

9/18 add reserve CB28, CB29 and stuff CB25, CB22, CB21 0.1uF

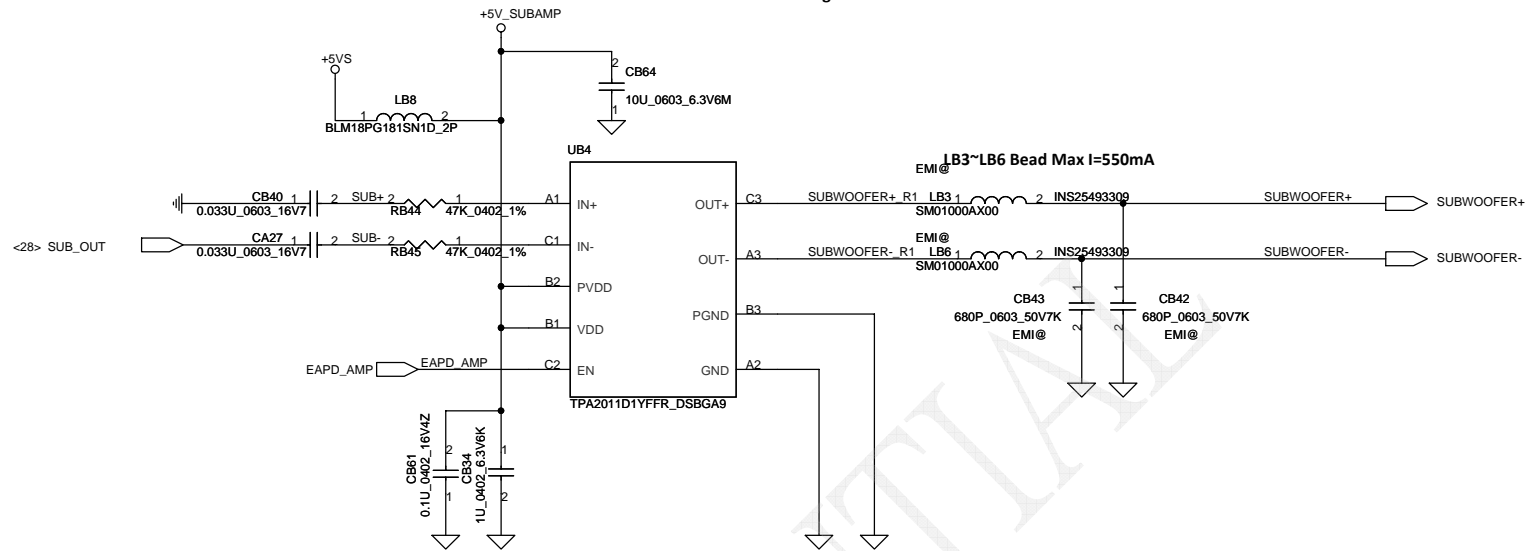


Check HP LDO PN

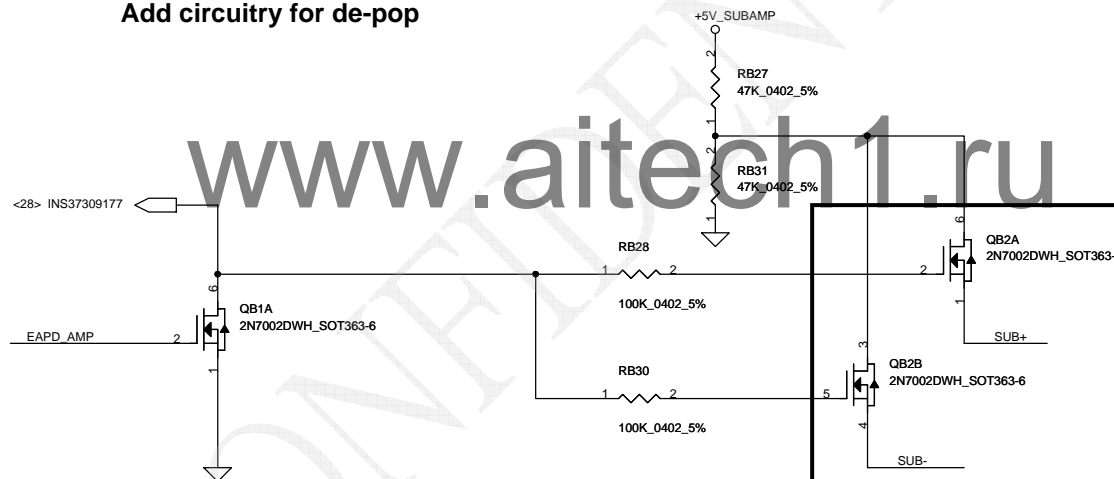
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Audio IDT 92HD91
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				Custom	LA-XXXXP
				Date	Sunday, July 08, 2013
				Sheet	28 of 60
				Rev	0.1

Subwoofer AMP TPA2011 = HPA01086YFFR

DB> TPA2012 Change to TPA2011



Add circuitry for de-pop



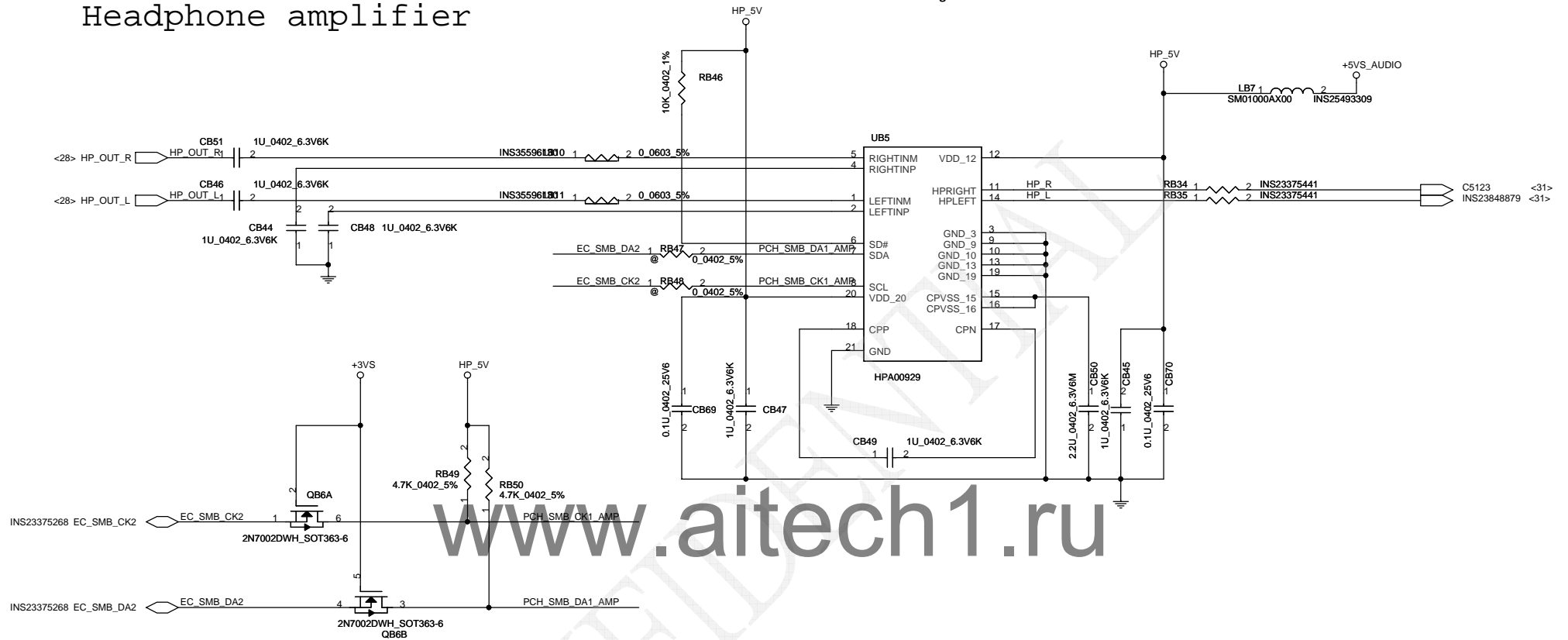
QB2 used Dual NPN BJT.
SB00000VH00 (METR3904KW)

Security Classification		Compal Secret Data				Compal Electronics, Inc.									
Issued Date		2011/06/29		Deciphered Date		2011/06/29		Title							
								15,22							
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								B		LA-XXXXP		0.1			
								Date:		Saturday, July 06, 2013		Sheet		29 of 60	

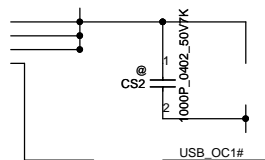
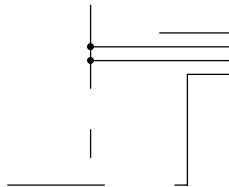
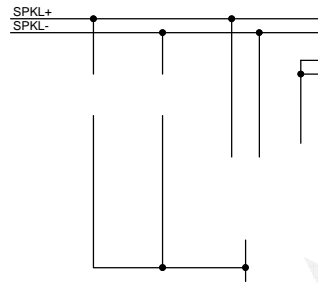
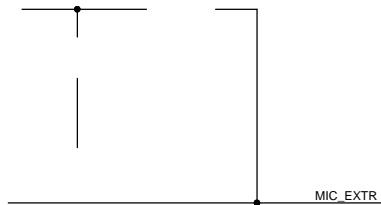
Headphone AMP TPA6130A2 = HPA00929

DB> HPA01196 Change to HPA00929

Headphone amplifier

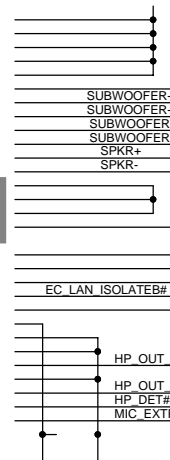


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Issued Date	2009/04/07	Deciphered Date	2012/10/21	Title	D:\ORCAD386\ORCAD\DC545\	
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				B	LA-XXXXP	0.1
				Date:	Saturday, July 06, 2013	Sheet 30 of 60



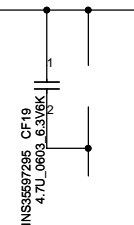
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EC LAN ISOLATEB#



EC LAN ISOLATEB#

HP OUT R 1
HP OUT L 1
HP DET#
MIC EXTR



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				Sheet	31 of 60
				Rev	0.1

PEG_HTX_C_GRX_P7
PEG_HTX_C_GRX_N7
PEG_HTX_C_GRX_P8
PEG_HTX_C_GRX_N8
PEG_HTX_C_GRX_P9
PEG_HTX_C_GRX_N9
PEG_HTX_C_GRX_P10
PEG_HTX_C_GRX_N10

GPU_GPIO0
GPU_GPIO6
GPU_GPIO8
GPU_GPIO9
GPU_VID0
GPU_THERMAL_DET#
PSI

GPU_THERMAL_DET#
GPU_GPIO6
PSI
GPU_GPIO8
GPU_GPIO9

TGL_GATE
GPU_GPIO0
FB_CLAMP
DGPU_PWR_EN#

PEG GTX C HRX P7
PEG GTX C HRX N7 CV2 DIS@ 1
PEG GTX C HRX P8
PEG GTX C HRX N8
PEG GTX C HRX P9
PEG GTX C HRX N9 CV6 DIS@ 1
PEG GTX C HRX P10
PEG GTX C HRX N10

PEG GTX HRX P7
PEG GTX HRX N7
PEG GTX HRX P8
PEG GTX HRX N8
PEG GTX HRX P9
PEG GTX HRX N9
PEG GTX HRX P10
PEG GTX HRX N10

GPU_JTAG_TCK
GPU_JTAG_TRST
TESTMODE

I2CA_SCL
I2CA_SDA
I2CB_SCL
I2CB_SDA
I2CC_SCL
I2CC_SDA
I2CS_SCL
I2CS_SDA

GPU_CLKREQ#_R
TESTMODE
GPU_JTAG_TCK
GPU_JTAG_TRST

I2CB_SCL
I2CB_SDA
I2CC_SCL
I2CC_SDA
I2CS_SCL
I2CS_SDA

XTALSSIM
XTALOUT
XTALIN

PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEX_TERM#
PLT_RST_VGA#
GPU_CLKREQ#_R

PLT_RST#
DGPU_HOLD_RST#
PLT_RST_VGA#

GPU_CLKREQ#_R
RV188 0_0402_5%

I2CS_SCL
I2CS_SDA

RV24 1 DIS@ 2 10M_0402_5%
XTALIN
XTAL OUT

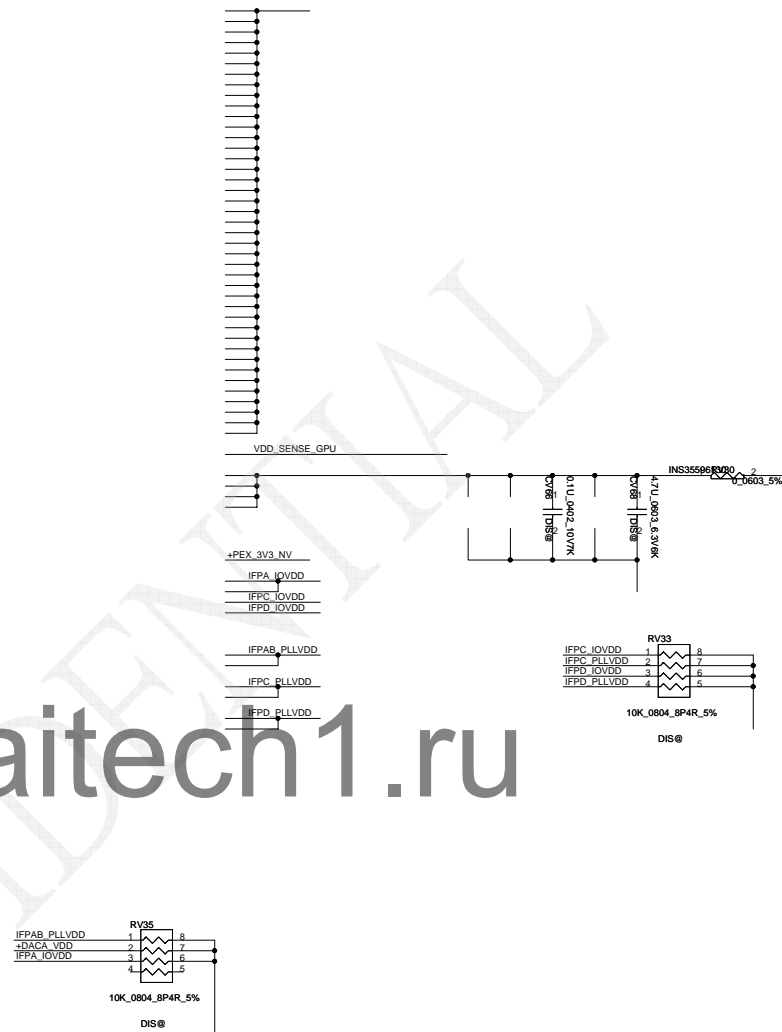
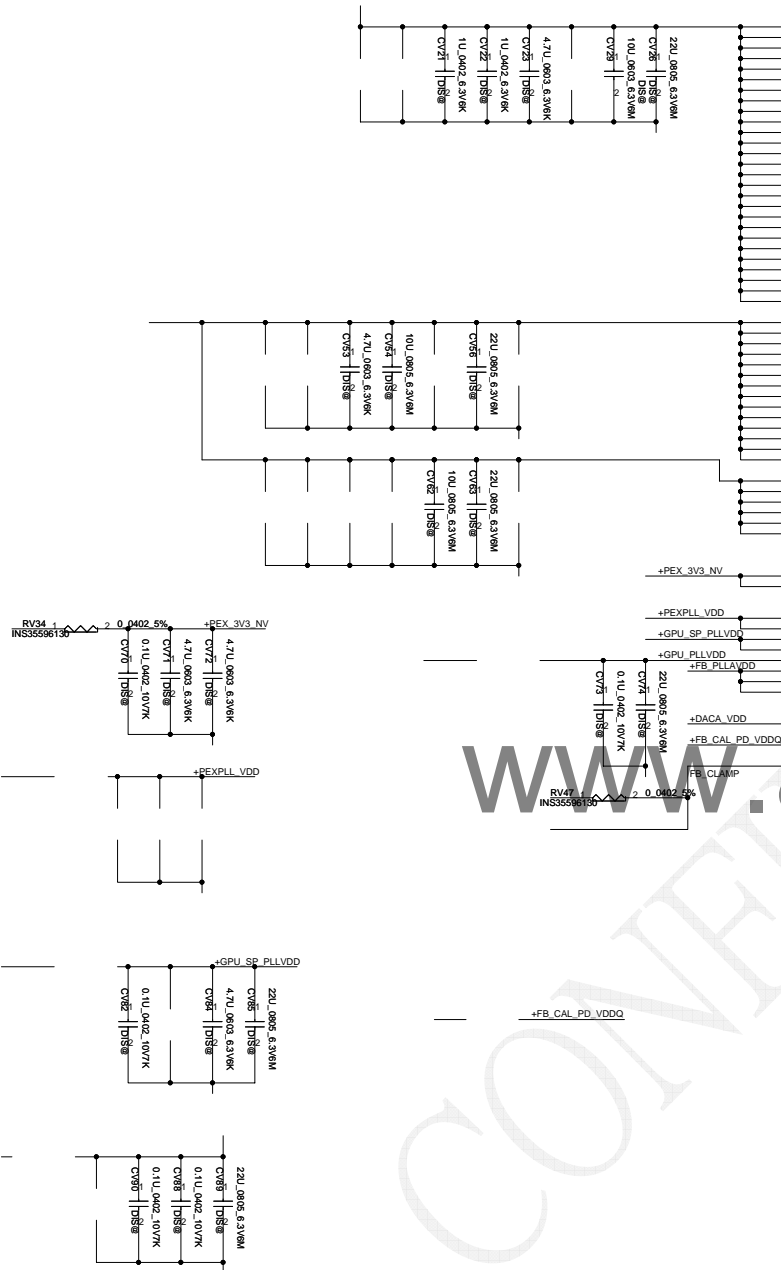
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Issued Date	INS16788846	Deciphered Date	WTEPHW1CIS SYMBOL HW RELEASE 2002-0628.OLB	Rev 1.0
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				INS47268555
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STRAP0 _____
STRAP1 _____
STRAP2 _____
STRAP3 _____
STRAP4 _____

ROM_CS _____
ROM_SCLK _____
ROM_SI _____
ROM_SO _____

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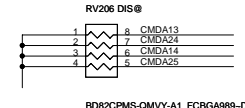
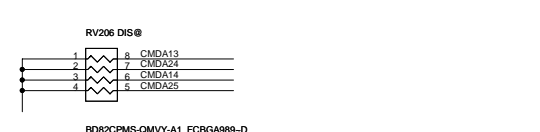
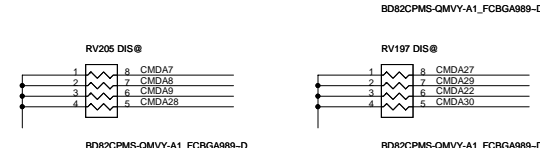
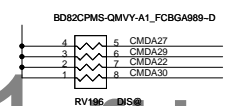
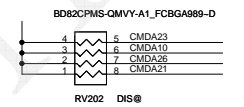
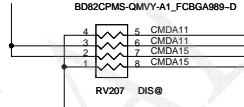
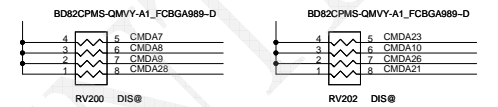
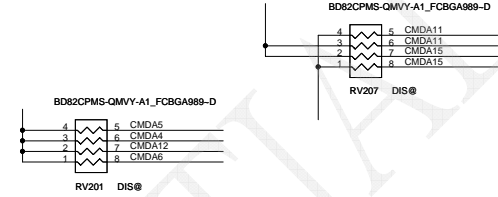
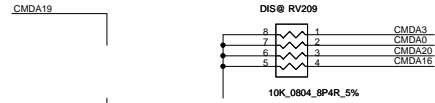
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		Date	Saturday, July 06, 2013	Sheet 35 of 60

MDA0
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DQSA7

T1405
CLKA0
CLKA0P
CLKA1
CLKA1P

RV137 1 2 2007/1/24 T-F 05:23:53
RV138 1 2 2007/1/24 T-F 05:23:53



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			INS35596872
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Data0~Data31

Rank 0

Rank 0



Group 1

Group 2

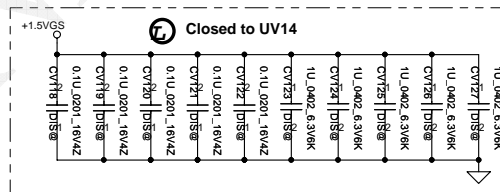
L:Group 0
H:Group 3

H:Group 3



Group 3

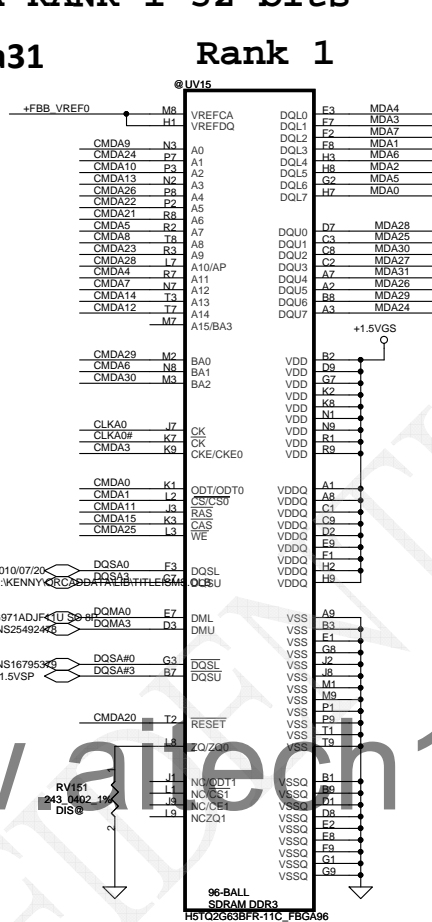
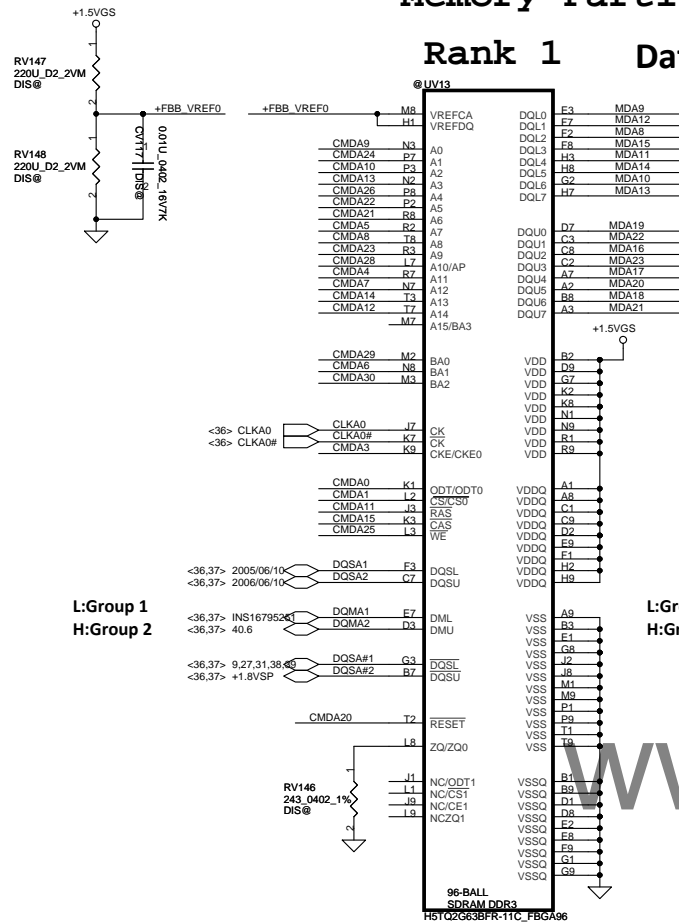
	RANK 0		RANK 1	
Address	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2



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Memory Partition A RANK 1 32 bits

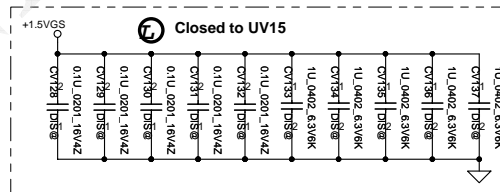
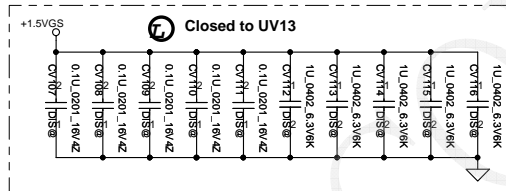
Rank 1 Data0~Data31 Rank 1



Group 0

Mode E - Mirror Mode Mapping

	RANK 0		RANK 1	
Address	0..31	32..63	0..31	32..63
FbX_CMD0	ODT_L		ODT_L	
FbX_CMD1			CS1#_L	
FbX_CMD2	CS0#_L			
FbX_CMD3	CKE_L		CKE_L	
FbX_CMD4	A9	A9	A11	A11
FbX_CMD5	A6	A6	A7	A7
FbX_CMD6	A3	A3	BA1	BA1
FbX_CMD7	A0	A0	A12	A12
FbX_CMD8	A8	A8	A8	A8
FbX_CMD9	A12	A12	A0	A0
FbX_CMD10	A1	A1	A2	A2
FbX_CMD11	RAS#	RAS#	RAS#	RAS#
FbX_CMD12	A13	A13	A14	A14
FbX_CMD13	BA1	BA1	A3	A3
FbX_CMD14	A14	A14	A13	A13
FbX_CMD15	CAS#	CAS#	CAS#	CAS#
FbX_CMD16		ODT_H		ODT_H
FbX_CMD17			CS1#_H	
FbX_CMD18		CS0#_H		
FbX_CMD19		CKE_H		CKE_H
FbX_CMD20	RST	RST	RST	RST
FbX_CMD21	A7	A7	A6	A6
FbX_CMD22	A4	A4	A5	A5
FbX_CMD23	A11	A11	A9	A9
FbX_CMD24	A2	A2	A1	A1
FbX_CMD25	A10	A10	WE#	WE#
FbX_CMD26	A5	A5	A4	A4
FbX_CMD27	BA2	BA2		
FbX_CMD28	WE#	WE#	A10	A10
FbX_CMD29	BA0	BA0	BA0	BA0
FbX_CMD30			BA2	BA2



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Rank 0



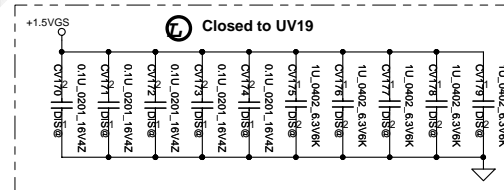
U1 Closed to UV18

Timing diagram for U1 (Closed to UV18) showing a sequence of 10 pulses. The pulses are labeled with their corresponding UV values: UV18, UV17, UV16, UV15, UV14, UV13, UV12, UV11, UV10, and UV9. The pulses are shown as high-level signals with varying widths. The diagram is titled "U1 Closed to UV18" and has a scale bar at the top indicating "+1.5VGS".

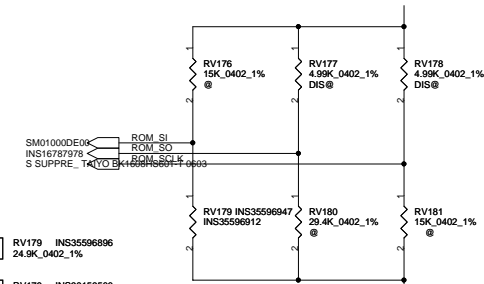
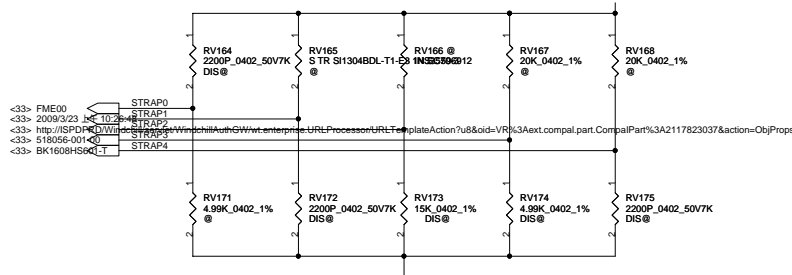
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Manufacturer P/N>



	RANK 0		RANK 1	
Address	0...31	32..63	0...31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18		CS0#_H		
FBx_CMD19		CKE_H		CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2

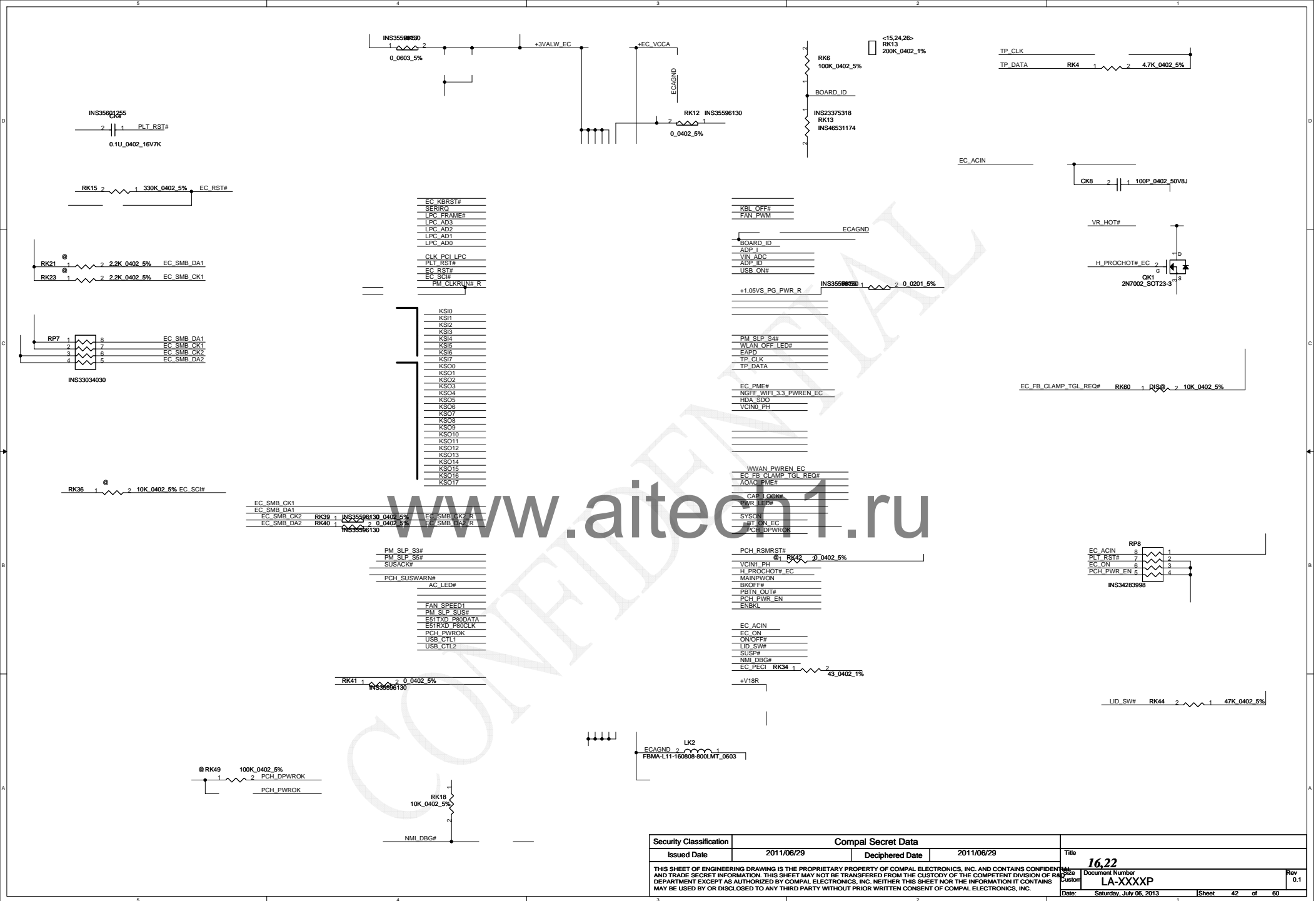


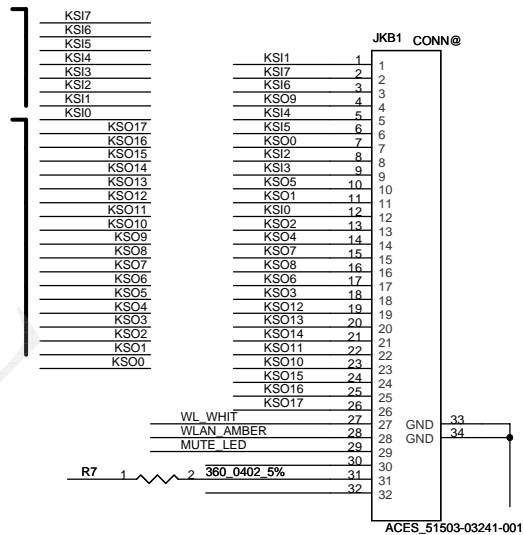
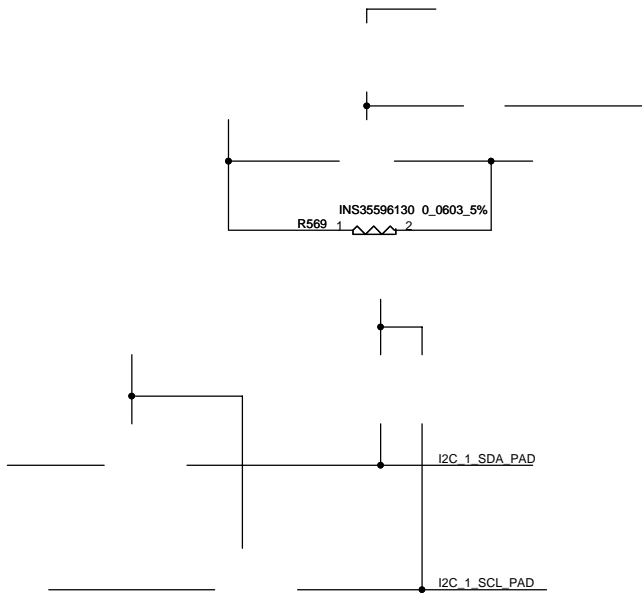
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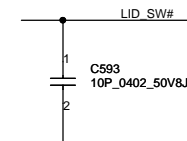
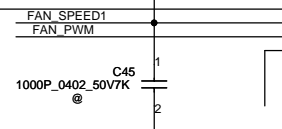
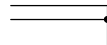
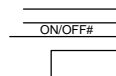
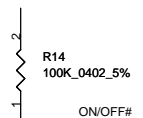
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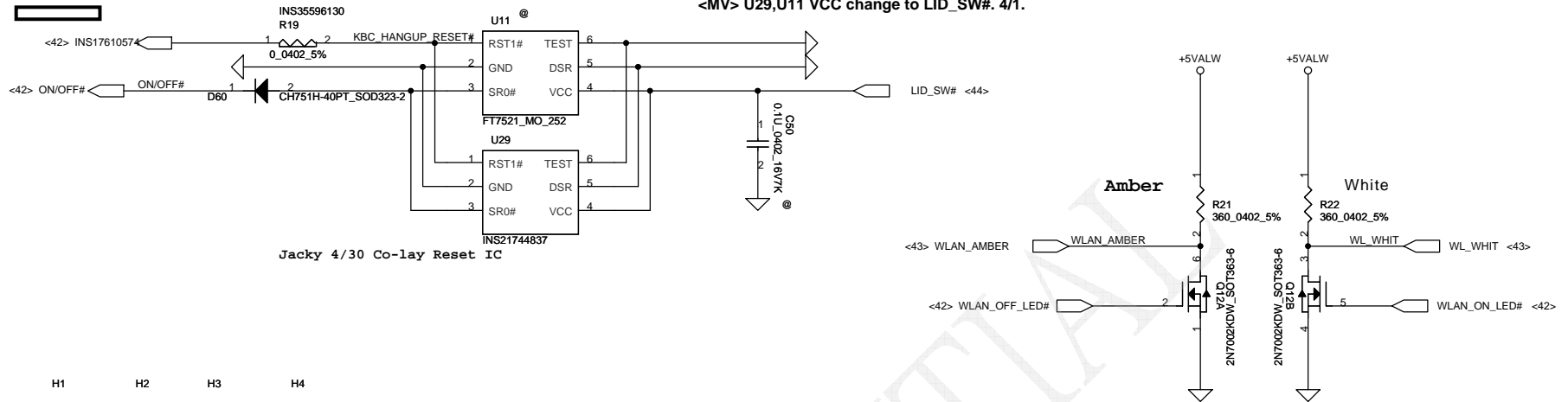
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				Date: Saturday, July 06, 2013	Rev 0.1
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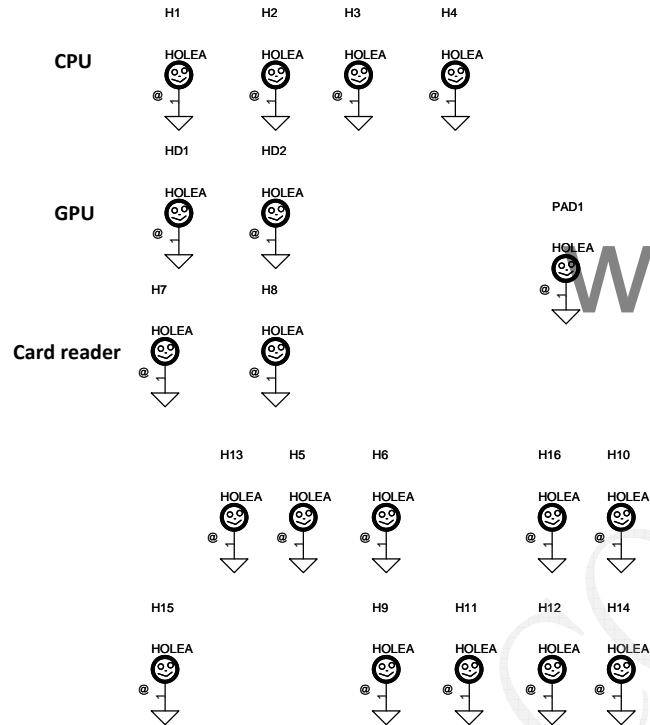
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 <MV> RST1# change to EC_RST#,4/10

Reset IC

<MV> U29,U11 VCC change to LID_SW#. 4/1.



WLAN_OFF_LED# & WLAN_ON_LED# must keep low(0V) when lamp all off.



PCB

LA-9314PR10:DA8000X6010

INS35596872
 INS47267858

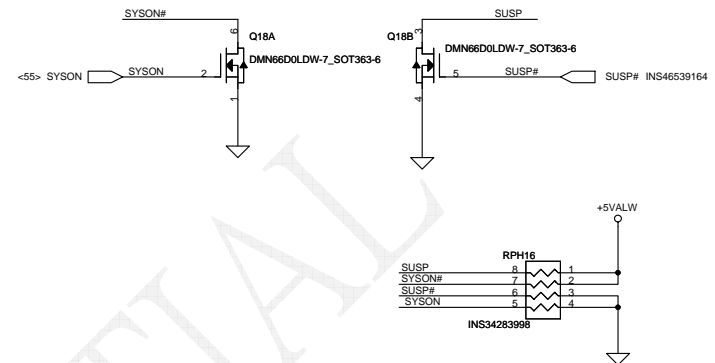
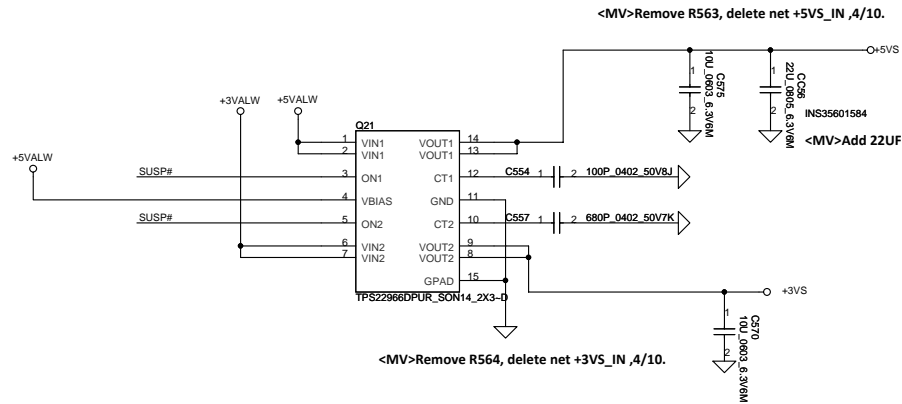
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Sensor hub -->G-sensor

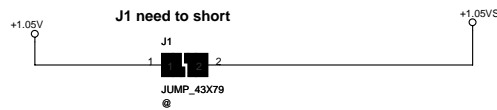


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				Date	Saturday, July 06, 2013	Sheet 46 of 60



+1.05V TO +1.05VS

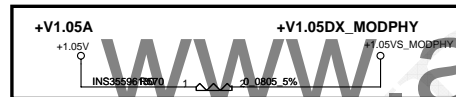


AO4430L
VGS Max=+/- 20V
VGS(Th) max=2.5V

Rds Max=5.5m @VGS=10V
Rds Max=7.5m @VGS=4.5V

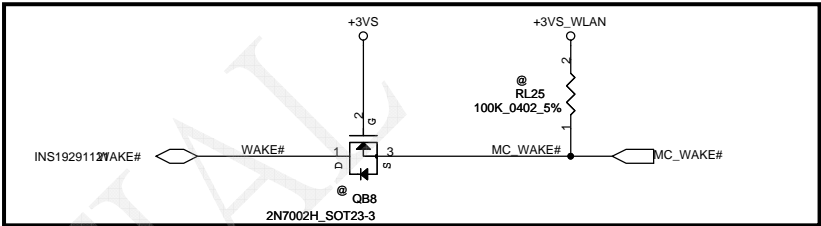
CPU +V1.05DX_MODPHY
Max Rdson <6m ohm
1840mA

AO4430L
VGS Max=+/- 20V
VGS(Th) max=2.5V
Rds Max=5.5m @VGS=10V
Rds Max=7.5m @VGS=4.5V



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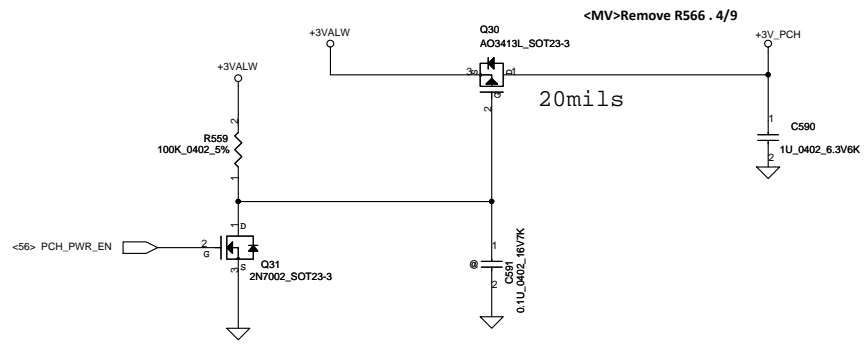
NGFF and WLAN



PV# 2013.01.23 Add Q8 abd RL25 to support OBFF
PV# 2013.02.22 Unpop Q8 and RL23 for not support OBFF

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<DB>NonCS no +1.8VS and low switch-->PMOS

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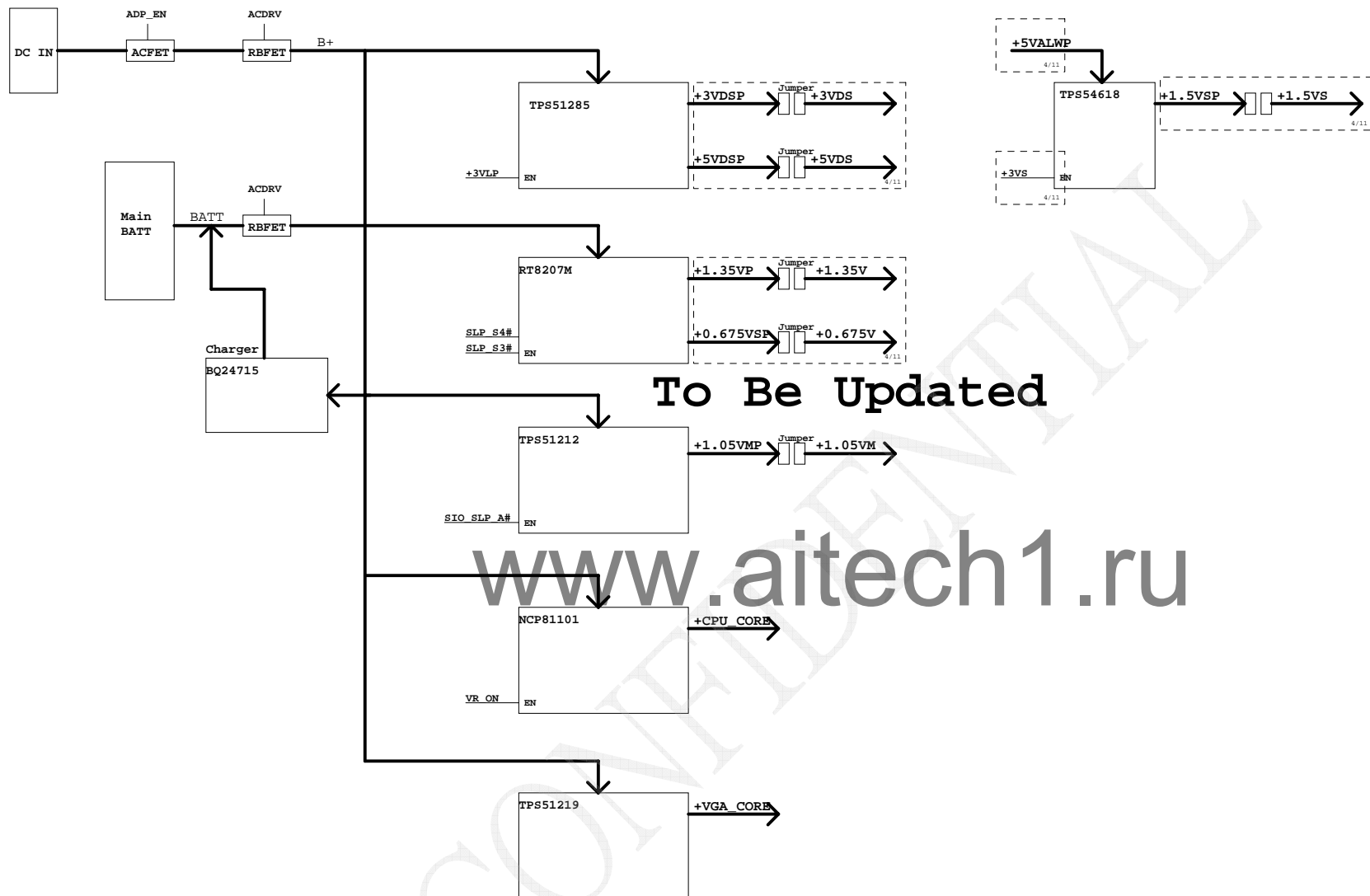
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Headphone and Mic conn

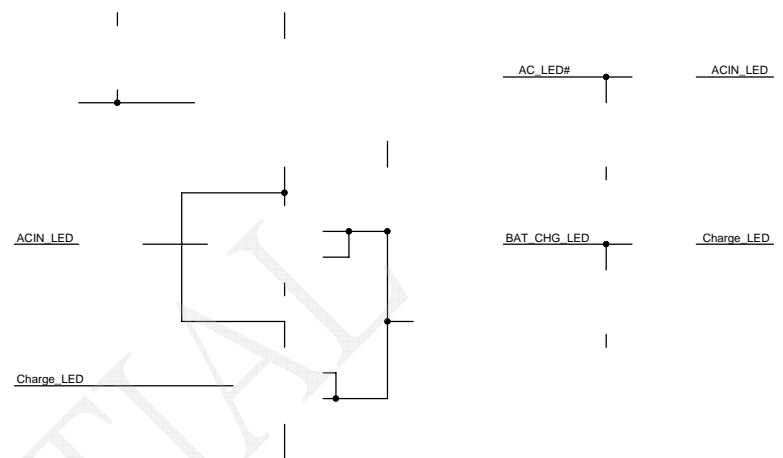
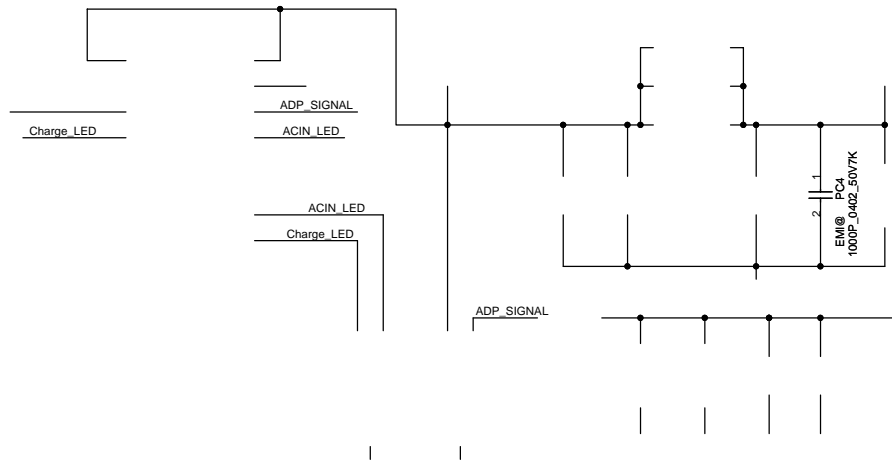
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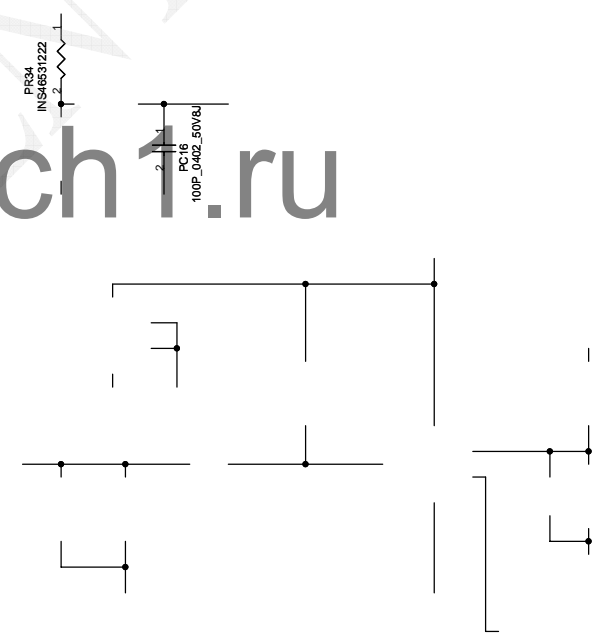
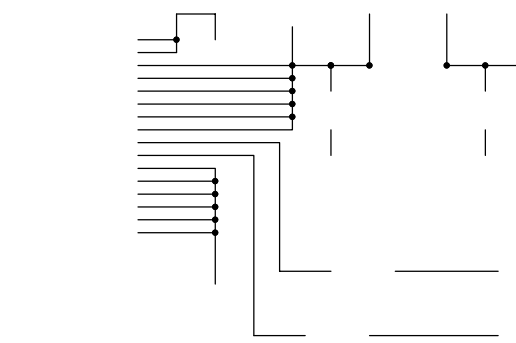
Compal Electronics, Inc.



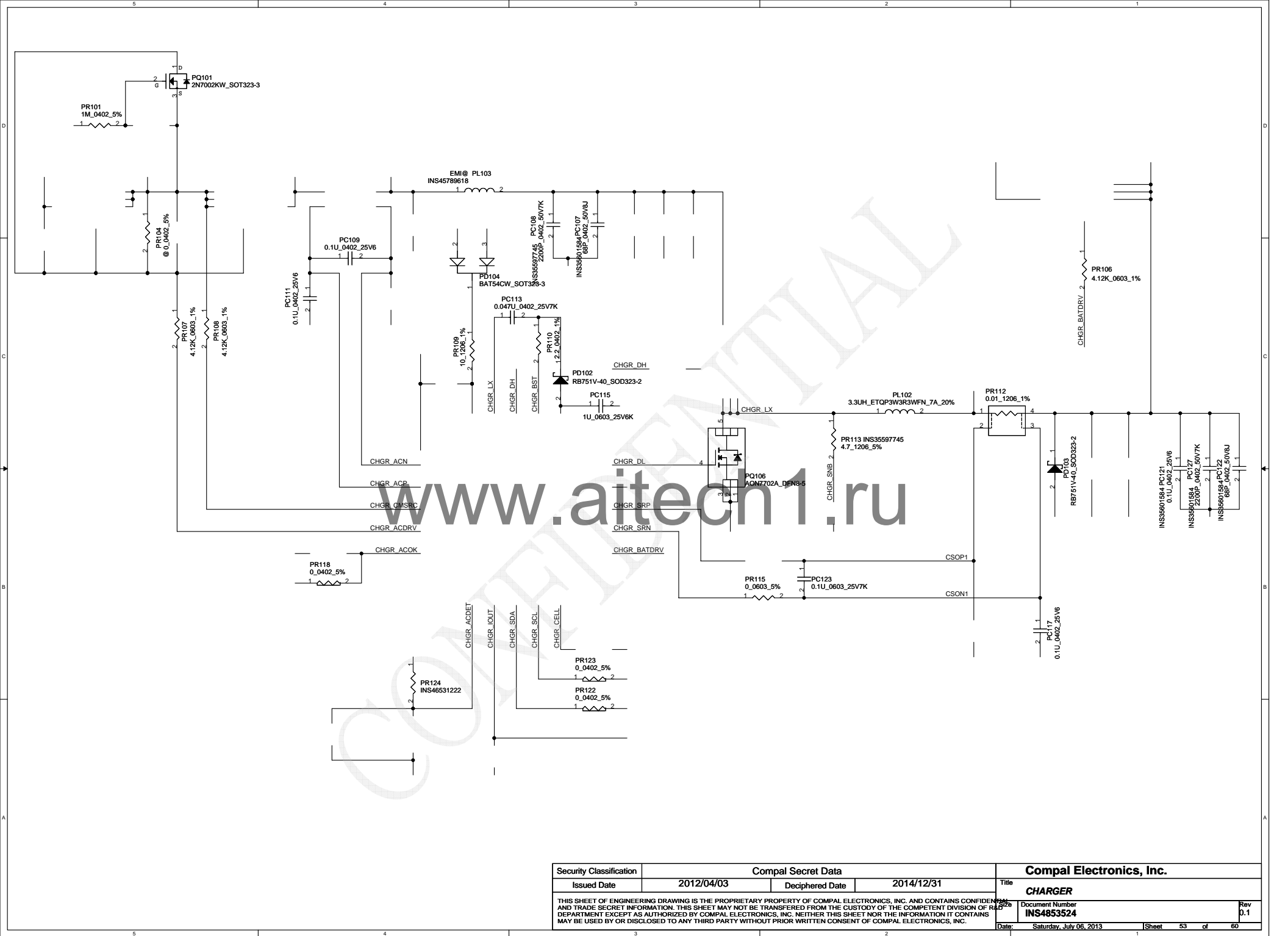
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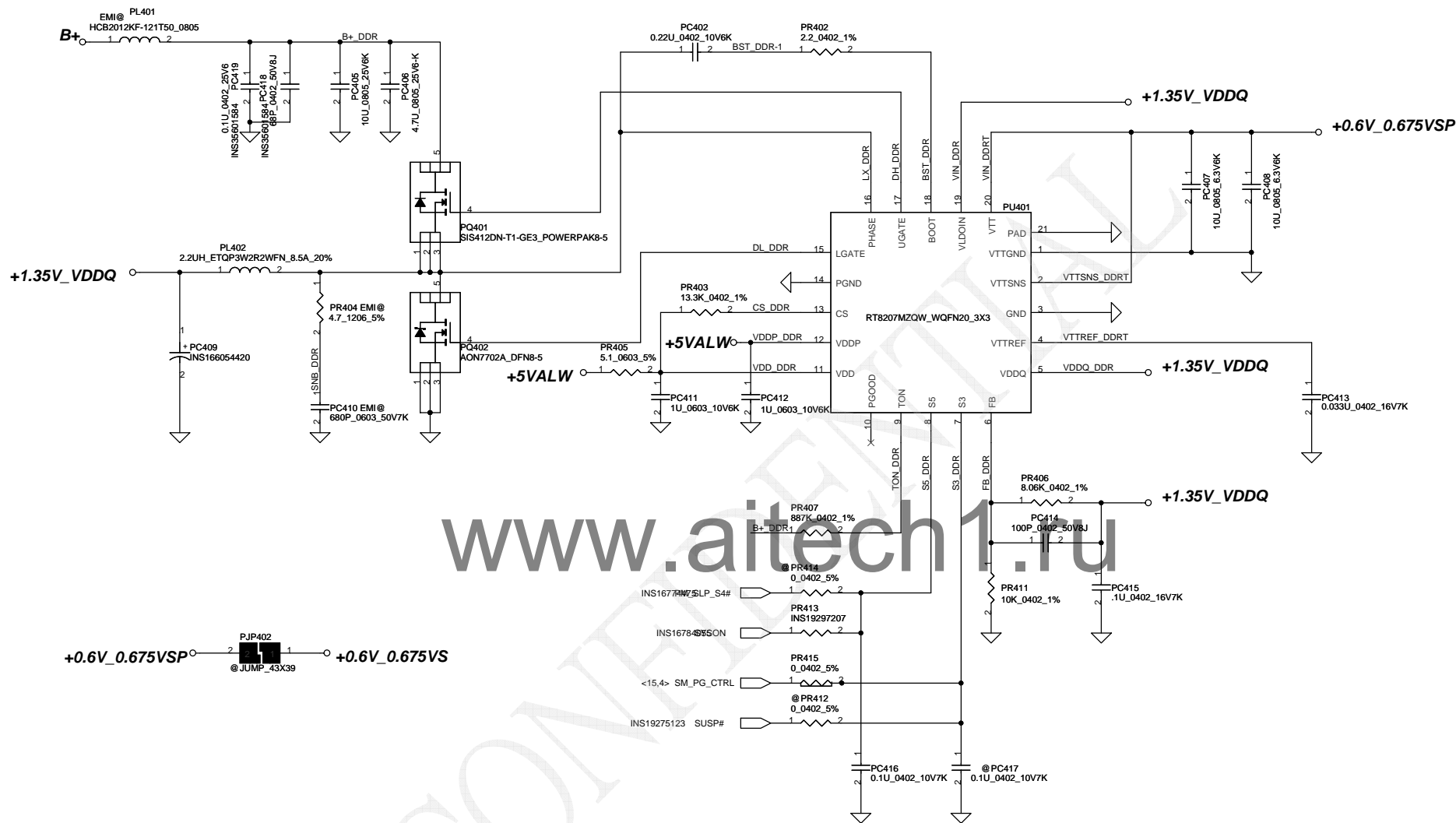
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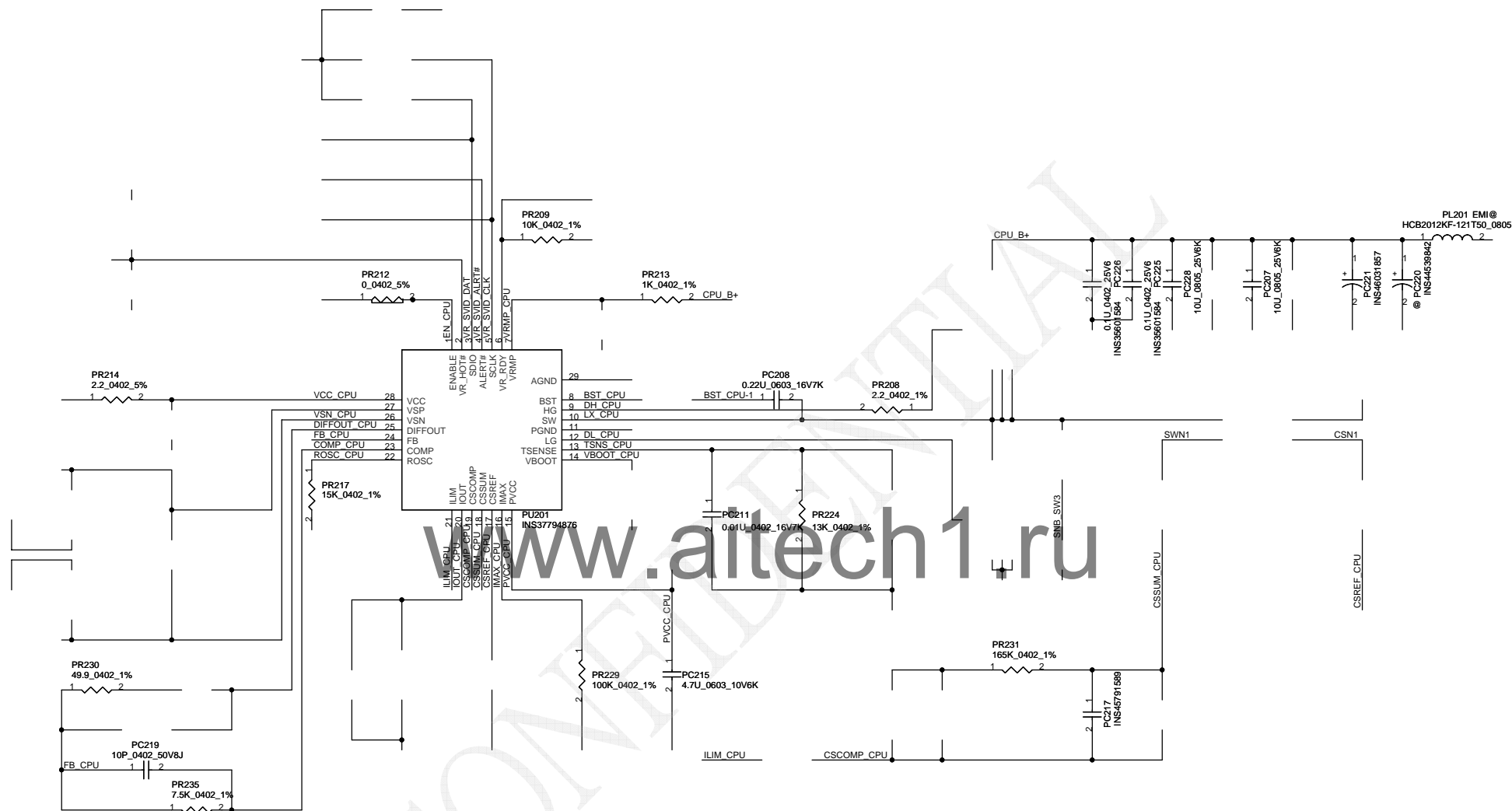
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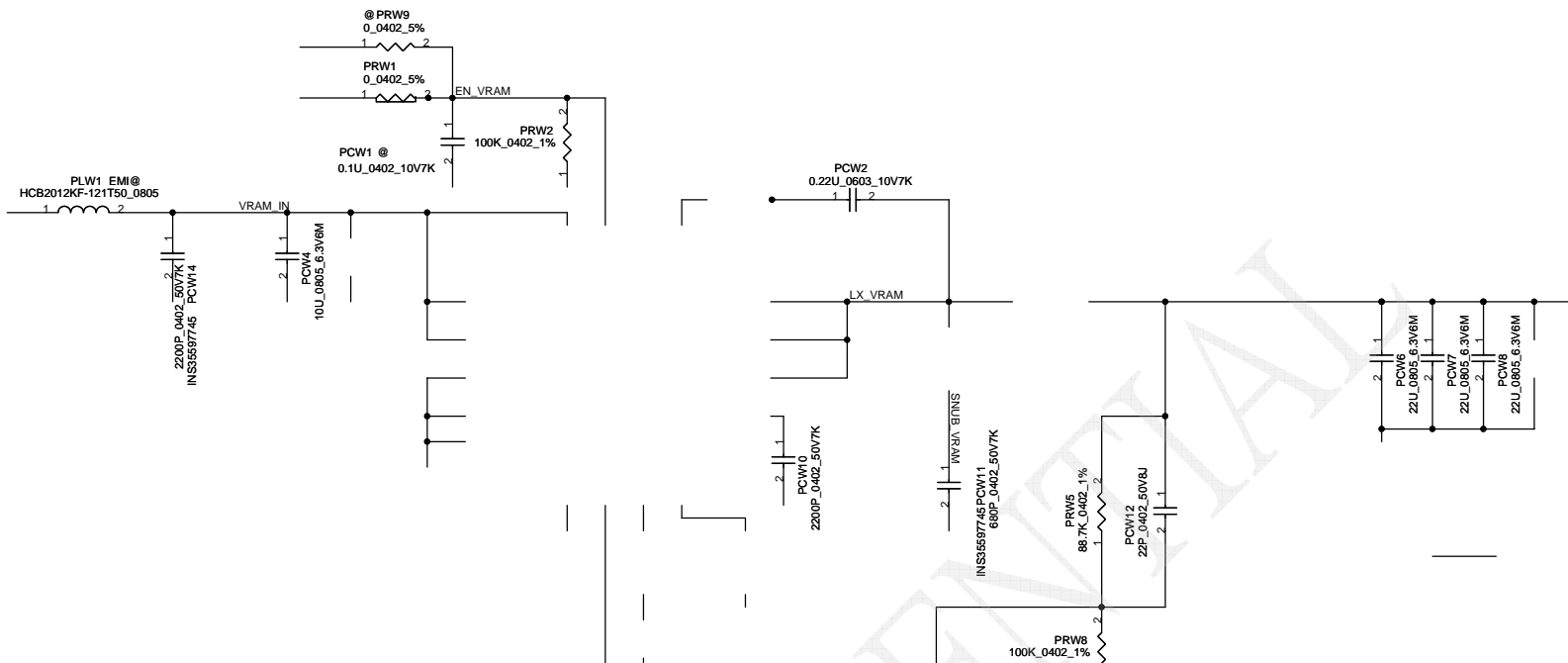
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			Date: Saturday, July 06, 2013	Sheet 55 of 60



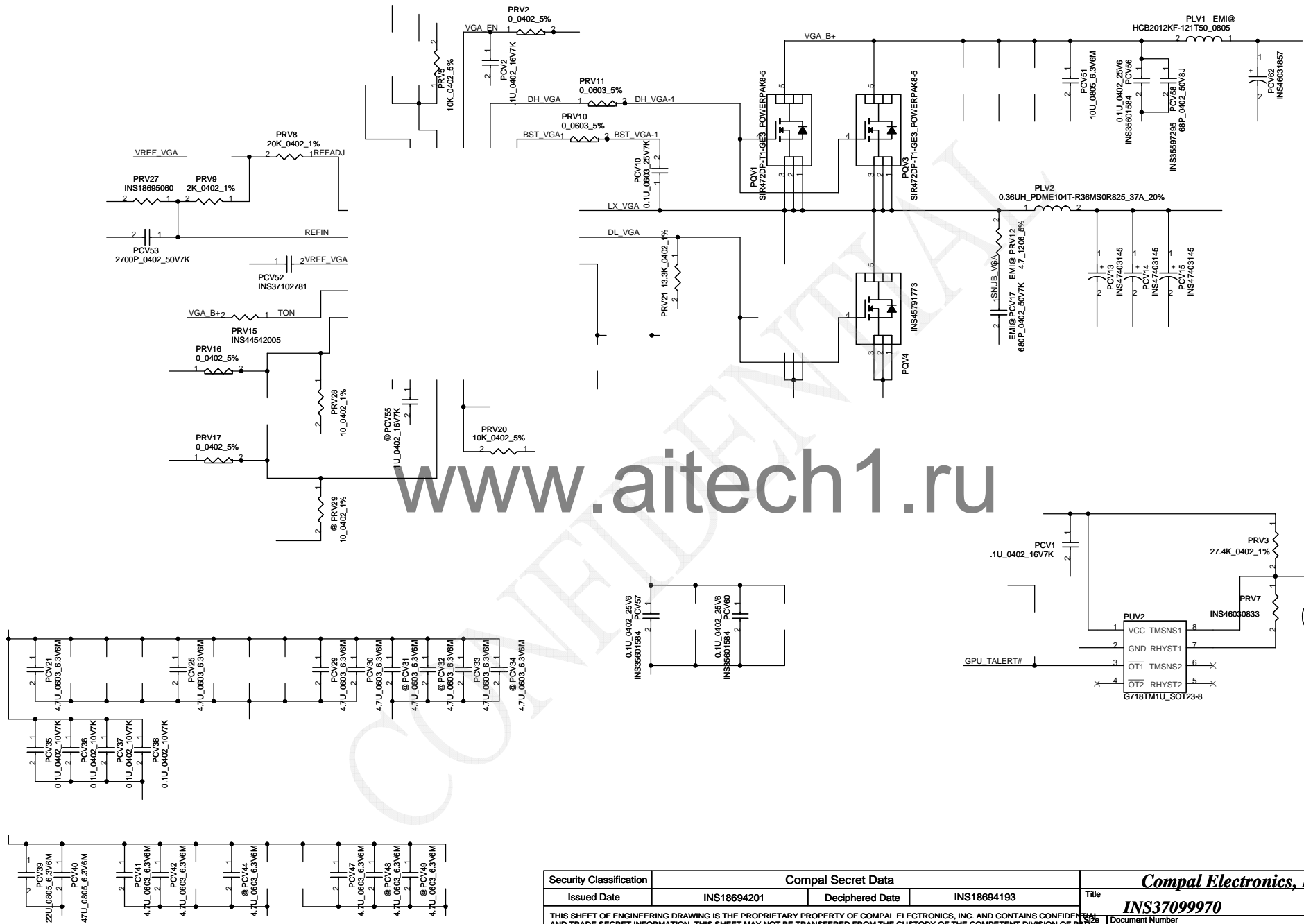
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